Altair PollEx 2021

PCB User Guide

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Conventions Used in this Guide

This guide uses the following conventions:

Bold Italic	All commands from the user interface. Options, menus, buttons, and dialog box names are bolded, but not italicized. Example: On the **Welcome** screen, click ***Next***.
`Courier`	The path of a program or folder; a web address; a file name or component; text that the user is expected to enter. Example: The default path is `C:\Program Files\Altair\2020\PollEx`

Questions regarding the document may be directed to PollEx team at PollEx_support_kr@altair.com.

PollEx Introduction

PollEx suite is knowledge-based design-verification toolset for PCB. It provides functions for all processes from concept design – schematic design – layout – verification(validation) – manufacturing to make them is most effectively used. In addition, it provides well customized environments which are widely used among various types of electronic process engineers. PollEx collects all functions which are used by design tools, manufacturing tools and process management solutions. With easy-to-use operation and versatile functions will guide users to the new electronic exploring.

1. PollEx PCB Concept

PollEx PCB can read ASCII files come from various types of ECADs or binary file having extension, PDBB. ASCII files from ECAD vendors are all different depending on ECAD suppliers. Users should know about the type of ECAD and their file extension before reading them into PollEx PCB program.

Below table shows PollEx PCB supporting ECAD vendors and their ASCII files.

ECAD Vendors	Products	File Extension	Version
Altium	PCAD	`*.pcb`	~PCAD 2006
	Protel	`*.pcb`	※~Protel 99 SE
	Designer	`*.PcbDoc`	~16.0
Cadence	Allegro	`*.comp, *.comppin, *.geom, *.lay, *.net, *.pad`	all
	APD	After changing *.mcm to *.brd, use Allegro reading method.	all
	Spectra	`*.dsn`	all
	OrCAD Layout	`*.dsn`	all
CADVANCE		`*.dsn, *.dbg, *.dbr`	all
Autodesk EAGLE		`*.brd`	all
Mentor Graphics	BoardStation	`*.geom, *.nets, *.comp, *.traces`	all
	BoardStation (Neutral)	`*.neutral, *.geom, *.trace`	all
	Xpedition	`Cell.hkp, JobPrefs.hkp, Layout.hkp, NetProps.hkp`	all
	PADS	`*.asc`	5.0~
(Valor)	ODB++	Folder	all
ZUKEN	CADSTAR	`*.cpa`	all

	CR5000 - Board Designer	Single board: `*.pcf, *.ftf` Arrayed board: `*.pnf, *.ftf`	7.0
	CR5000 - PWS	`*.bsf, *.ccf, *.mdf, *.udf, *.wdf`	all
IPC2581B		`*.xml`	all
CAM350		`*.cam`	all
Gerber	RS-274D	-	all
	RS-274X	-	all
PollEx	PollEx PCB (Binary)	`*.PDBB`	3.0~
	PollEx PCB (ASCII)	`*.pdba`	4.0~
	PollEx PCB	`*.pdbx`	2020

※The extension of Altium Protel 99 SE is same with *.pcb, but the format is the same as Altium Designer. So, user should import ASCII file with using 'Altium Designer' menu.

If user has other formats which are not supported by PollEx PCB, users can be supported by UCS(User Customizing Service).

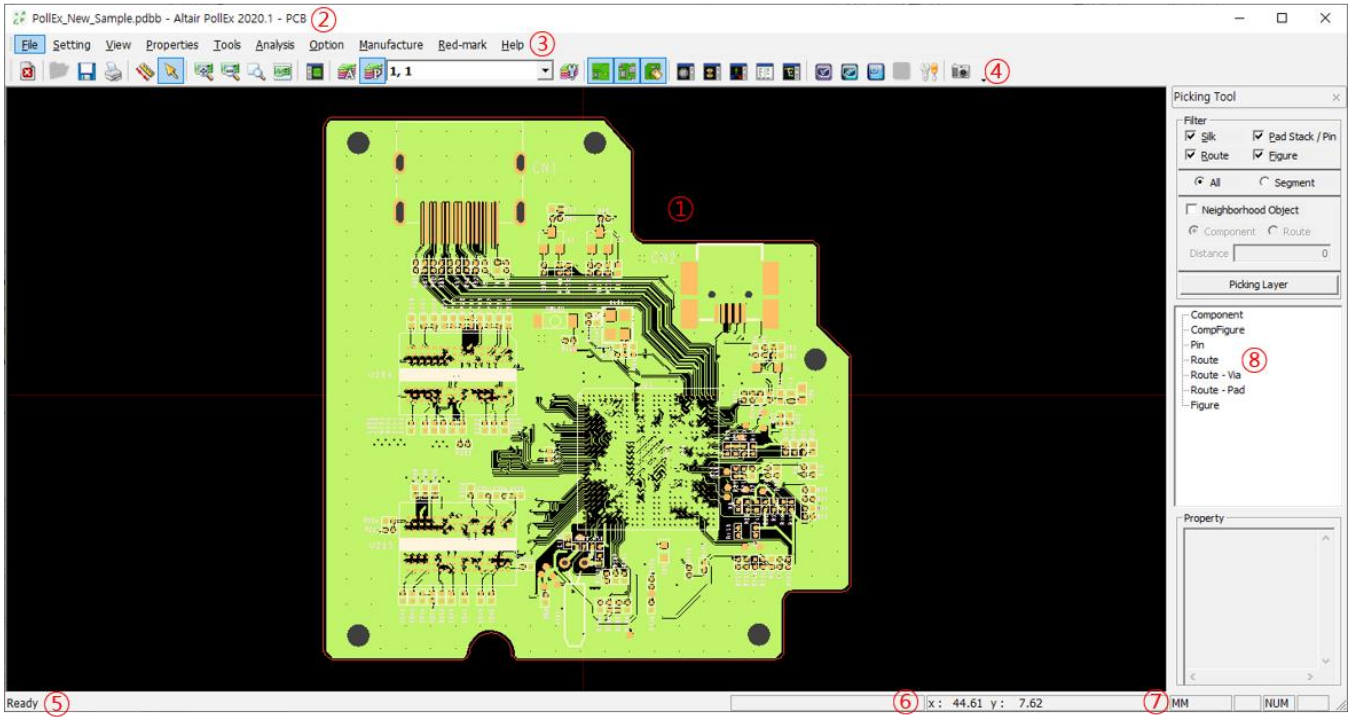
2. PollEx PCB Launching

Launch the menu, `Start\Altair\2020\PollEx\PollEx_Launcher.exe`.

Launch from the directory, `C:\Program Files\Altair\2020\PollEx\PollEx_Launcher.exe`.

3. PollEx PCB Windows

Below picture is the launched PollEx PCB main window.



① Users can review the layout design at here, main window viewing area.
② At the top of main frame window, user can see the version of PollEx PCB and active file name and path.
③ Menu Bar gives users many useful functions.
④ Tool-Bar menu gives users easy and institute icon menu.
⑤ Status-Bar menu shows current application status.
⑥ PollEx PCB shows the location of mouse cursor point.
⑦ Show the unit of active PCB layout design.
⑧ Picking-Tool box show the information of mouse-selected objects.

4. PollEx Menu Structure

PollEx PCB has 8 menus in menu bar. They will guide user to easily explore PCB layout.

Menu	Sub-menu	Shortcuts	Description
File	Import ECAD		Read various types of ECAD.
	Export to		PDB ASCII(`*.pdba`), PDB XML(`*.pdbx`), EDA Vender's Format, Restricted PDBB, DXF, GDSII
	Open PDB Binary File	Ctrl+O	Open saved PollEx PCB file.
	Save	Ctrl+S	Save into PollEx PCB file.
	Save As		Save as different name PollEx PCB file.
	Save As Project		Create project folder for data handling in case of SI/Thermal analysis.
	Print	Ctrl+P	Print into paper or Bitmap/Postscript image.
	Close		Close active working.
	Recent PDBB File List		List out and read recently imported file.
	Exit		Exit from PollEx PCB.
Setting	Environment		Set default PollEx PCB using environments.
	Layer	Alt+L	Set/View PollEx PCB's layer status.

	Measure		Measure the distance between objects.
	Picking		Check the properties of objects.
	Unit Conversion		Change the unit of PCB layout.
	Board Information		See the whole board information.
View	Previous		Go back to previous viewing status(under construction).
	Next		Go to next viewing status(under construction).
	Zoom In	+, wheel ↓	Zoom in viewing status.
	Zoom Out	-, wheel ↑	Zoom out viewing status.
	Zoom Window	Alt+W	Zoom in for mouse two picking points.
	Zoom 1:1	Alt+1	PollEx PCB default design viewing status.
	Toggle 1:1	Ctrl +Tab	Go to default window and shows previous Zoom in area.
	Set Capture Window	Mouse Click & Ctrl+C	Save mouse clicked area into system buffer.
	Mirror View	Ctrl+M	Shows mirrored PCB image.
	Board Rotation		Rotate PCB for given rotation angle.
	Route On/Off		Toggle for displaying routing pattern On/Off.
	Component On/Off		Toggle for displaying component On/Off
	Polygon Fill		Toggle for displaying polygon Fill/UnFill
	Display Setup		Set status for displaying route/via/component.
	Net Display On/Off		Toggle for displaying net On/Off.
	Board Mini-Map		Show current viewing area regarding to whole PCB layout area.
	Menu Bar		Toggle for showing menu-bar On/Off.
	Tool Bar		Toggle for showing toolbar On/Off.
	Status Bar		Toggle for showing status-bar On/Off.
Properties	Nets		Show netlist and nets' properties.
	Composite-nets		Show all composite nets' properties.
	Net Classes		Show all net classes
	Net Buses/Group		Show all Buses/Group
	Parts		Show partlist and linkage status with local part library.
	Components		Show component list and assign passive component type.
	Material Library		Show materials' properties.
	Layer Stack		Show/Edit PCB layout Stack-Up.
	Rigid-Flexible PCB		Define the flexible PCB area
Tools	Find /Query	Alt+Q	Find or query for component and net.
	PCB Explorer	Ctrl+F	Explore components, nets or combinations.
	Change Reference Names		Change reference names.
	Change Board Origin		Change the origin point of PCB design.
	Go to Location	Alt+G	Move cursor point to the given location.
	Component Arrangement Plan		Show the components' placement status.
	PCB Data Extractor		Make document regarding components or

			nets.
	Extact Decap Data		Make list for decoupling capacitors on PCB.
	Net Color		Change/Save colors of routing nets.
	Net Length View		Make list for all nets' length.
	Net Analyzer		Make analyzing report for all nets on PCB.
	Change Net Name		Change net name with using ruf file.
	Thermal Resistance Calculator		Calculate thermal resistance.
	Gerber Transformation		After reading Gerber file, change the origin of Gerber layers to fit with PCB design.
	Visual Layer Composition		Make user specific layers' composition.
	BOM Changer		Change ECAD Part Name based on BOM data.
	Worksheet Planner		Launch Worksheet Planner tool.
	Golden Sample		Launch Golden Sample tool.
Analysis	Signal Integrity		Launch Signal Integrity analysis tool.
	Power Integrity		Launch Power Integrity analysis tool.
	Radiated Emission		Launch Radiated Emission analysis tool.
	Thermal		Launch board level thermal analysis tool.
Option	Part Viewer		Parts viewer for all parts used in PCB design.
	Real PCB Assembly Viewer		3D assembled PCB viewer using 3D package link. Also provide the exporting to STEP.
	Net 2D/3D Viewer		Show routing nets' structure with 2D/3D.
	Padstack/Via Viewer		Padstack/Via viewer for all used in PCB design.
	Net Topology Viewer		Show net structure as topology style.
	DFM		Design For Manufacturing
	DFE		Design For Electronics
	DFE+		Design For Electronics Plus
	DFA		Design For Assembly
	DFx Core Running		Define the DFx input files
	Attribute Finder		Make property list for components and their pins.
Red-mark	Red-mark		Feature to make comment on PCB design.
	Red-mark Plus		Advanced feature of PCB design mark-up
Help	PollEx Manual	F1	Open PollEx PCB manual.

5. PollEx PCB Tool Bar

PollEx PCB provides toolbar for frequently used menus.

① File management functions
- Close: Close active design.
- Open: Open PDBB file.
- Save: Save active design into PDBB file.
- Print: Print current view status into paper or Bitmap/Postscript image.

② Measure/Picking tools
- Provide the function to measure objects or find the properties of objects. Two dialog menus run as toggle mode.
- Picking tool: For mouse selected objects, show all related properties on picking dialog box.
- Measure tool: Measure objects' size or distance between various objects.

③ View control menu
- Zoom In/Zoom Out
- Window Zoom: Zoom area for mouse selected two points.
- Zoom 1:1: Go back to default view status.

④ PCB Explorer
- Using PCB Explorer, user can search components or nets and component/net composition.

⑤ Layer Control
- Artwork Layer: View layers with artwork layer order.
- Physical Layer: View layers with physical layer order.
- Layer: For selecting layers, user can change layer viewing status or layer properties.

⑥ Object Display On/Off Control.
- Routing Data On/Off: Display On/Off function for route pattern.
- Components Data On/Off: Display On/Off function for components on PCB.
- Polygon Fill/Unfill: Display polygon or copper fill/unfill function.

⑦ Object Viewers/ Data Extraction Tool.
- Parts Viewer: See all parts used in PCB layout.
- Padstack/Via Viewer: See all padstacks and vias used in PCB layout.
- Net 2D/3D Viewer: See all routing nets on PCB layout.
- PCB Data Extractor: Documentation tool for nets or components and their related properties and objects. After making table, user can extract table information into MS/Excel sheets.
- Net Topology Viewer: Show net routing structure with topology style.

⑧ DFM Core Running
- Using this function, user can run PollEx DFM checking after specifying multiple DFM input files.

⑨ DFE Core Running

- Using this function, user can run PollEx DFE checking after specifying multiple DFE input files.

⑩ Metal Mask Manager
- Using this function, user can checks whether a PCB design uses a standard metal mask.

⑪ Board Information
- Window menu provide all information of working PCB. At dialog window, user can see file path, file generation date, board size, number of used component and nets… etc.

⑫ Capture
- Using this menu, for selecting region with two points mouse picking and shortcut key**, Ctrl+C**, user can easily get image file on PCB.

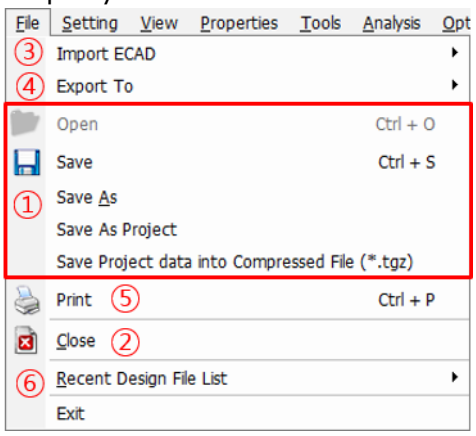
6. Mouse Control

To efficiently operate, PollEx PCB provides some useful mouse operations.

1) Window zoom control: Zoom In/Out, mouse wheel up/down.
2) Panning: Window scroll, mouse right button click + Move.
3) Picking: use mouse left button. And if picking tool is active status, all selected objects' information will be shown on picking tool.

File

Here, user can check basic functions, importing ECAD files into PollEx PCB and exporting working design to 3rd party EDA vendors' format.



① File Open and Save
- **Open**: Import PollEx PCB's binary file, `*.PDBB`.
- **Save** / **Save As**: Save active design into `*.PDBB` or different name of PDBB file.
- **Save As Project**: Create folder for data handling.
- **Save Project data into Compressed File (*.tgz):** Save the all of the current project data directory as a compressed file.

② File Close and Program Exit
- **Close**: Close working job file.
- **Exit**: Close PollEx PCB program.

③ Import ECAD
- Import design from ASCII file which are created by other EDA vendors' CAD tools. PollEx PCB supports various types of prominent ECAD vendors' format.

④ Export To
- **PDB ASCII (`*.pdba`)**: User can save and export the design file with the ASCII format.
- **Restricted PDBB**: User can save and export the design file with the user defined information.

⑤ Print
- PollEx PCB can print active window image into printer or images like bitmap or postscript style.

⑥ Recent PDBB File List
- import design from recently opened lists.

1. File Open / Save

PollEx PCB's binary data file has PDBB extension. After reading ASCII file from ECADs using PollEx PCB, user can save or import these files into PollEx PCB.

- Using the menu, **File > Open** with PDB Binary File (Shortcut key: **Ctrl + O**).

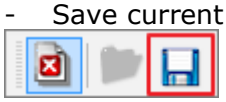
- Using the menu, **Recent PDBB File List**

Upon selecting design from recently used PDBB file list, user can easily open file. If user did not save design file or unstably closed case, the design file is not stored into the recent file list.

- **Save / Save As**

Use this menu to save current design to PDBB file. The one of merits of PDBB file is small file size compare to original ECAD design file. So, sending design to others or management will also be easy and fast without any loss of information.

- Save current design using the menu, **File > Save/Save As** (Shortcut key: ***Ctrl* + *S***).



2. File Close and Program Exit

User can use this menu to close active design or exit from PollEx PCB program.

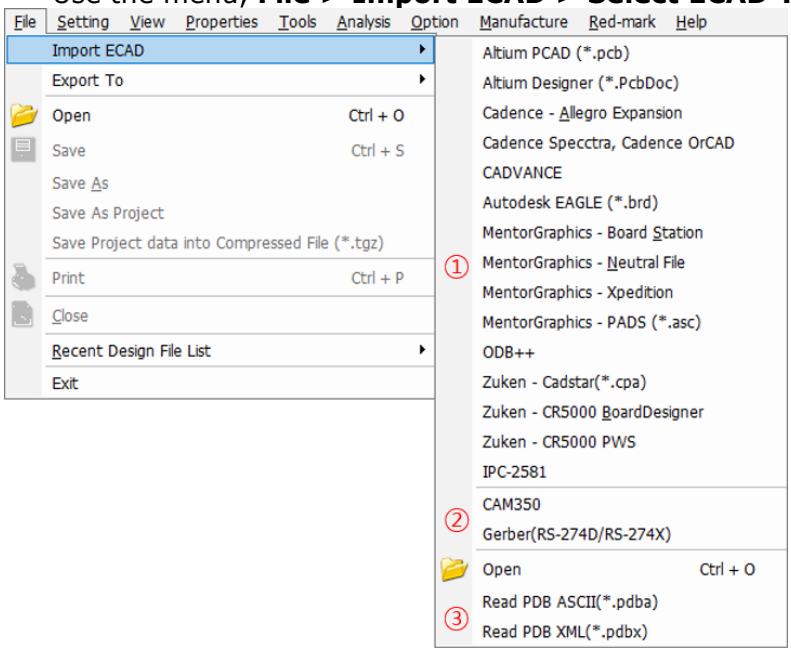
- Close active design using the menu, **File > Close**.

- Exit from PollEx PCB using the menu, **File > Exit**.

3. Import ECAD

All ECAD tools have their ASCII structures to be used by the 3rd party applications. PollEx PCB can import those ASCII files from various ECAD vendors. Depending on different types of ECAD ASCII files, this manual provides the way of importing them.

- Use the menu, **File > Import ECAD > Select ECAD Tool** to read ECAD's ASCII file.



① ECAD vendor lists which PollEx PCB can import.

② CAM350, Gerber file importing menu.
The purpose of GERBER file reading is to compare GERBER to PCB layout design. So, the number of readable GERBER layers have limitation in PollEx PCB. As the purpose of reviewing GERBER file, PollEx CAM is recommended.

③ ASCII, XML File importing menu, generated by PollEx PCB.

- User also can access the **Import ECAD** menu from **Right-mouse click > Pop-up window> Select ECAD Tool**.

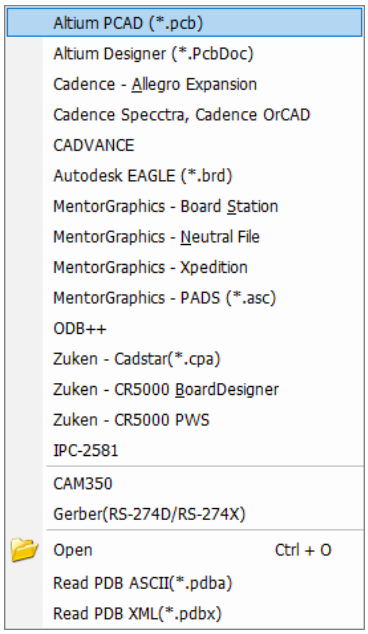
3.1. Altium PCAD/Designer Interface

PollEx PCB supports various Altium's PCAD, Protel and Designer files.

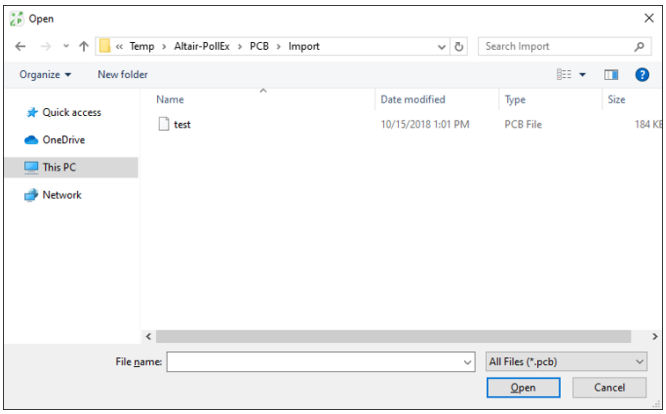
3.1.1. Altium PCAD

Step1. Extract PCAD ASCII file, `*.pcb` in Altium PCAD.

Step2. Use the menu, **File > Import ECAD > Altium PCAD**.



Step3. At file selection dialog box, select the target ASCII file, `*.pcb` to import it.



There is a format to import Altium PCAD as below.

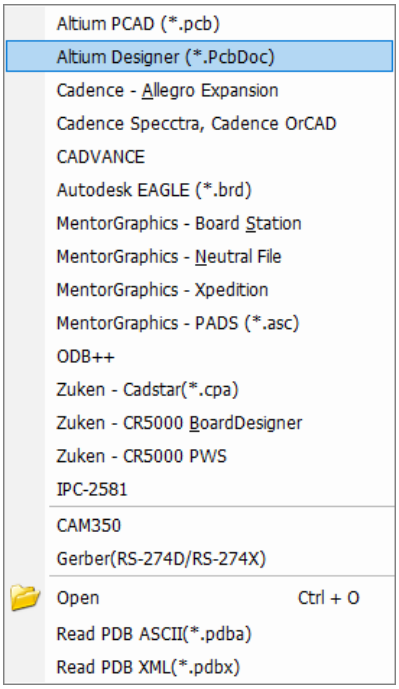
[Example of `*.pcb`]

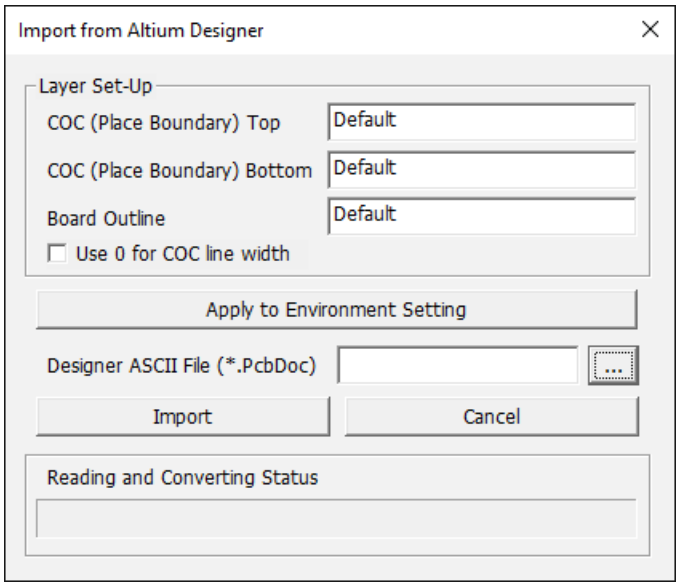
```
ACCEL_ASCII "F:\Temp\accel_demo.pcb"

(asciiHeader
  (asciiVersion 2 2)
  (timeStamp 1998 6 4 9 35 21)
  (program "ACCEL P-CAD PCB" "13.00.38")
  (copyright "Copyright © 1997 ACCEL Technologies, Inc.")
  (fileAuthor "T. Luong")
  (headerString "License: 4172-3005 150738 Wolfgang Schenke Router Solutions ")
  (fileUnits Mil)
)

(library "Library_1"
  (padStyleDef "(Default)"
    (holeDiam 38.0)
    (StartRange 1)
    (EndRange 2)
    (padShape (layerNumRef 1) (padShapeType Ellipse) (shapeWidth 60.0) (shapeHeight 60.0) )
    (padShape (layerNumRef 2) (padShapeType Ellipse) (shapeWidth 60.0) (shapeHeight 60.0) )
```

3.1.2. Altium Designer

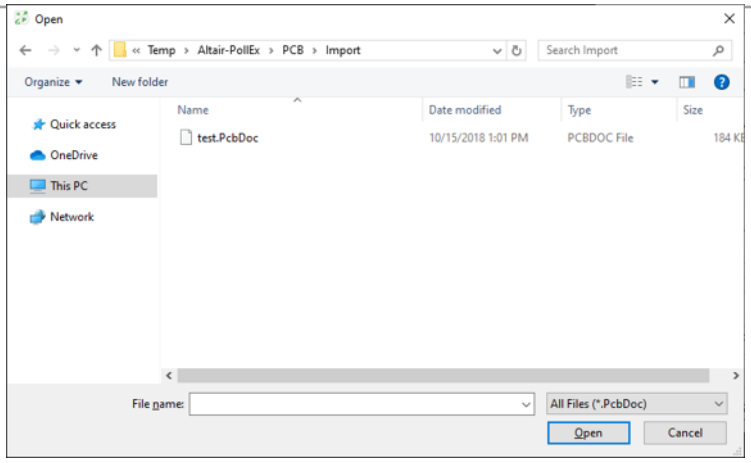
Step1. Extract Altium Designer ASCII file, `*.PcbDoc` in Altium Designer.

Step2. Use the menu, **File > Import ECAD > Altium Designer**.





Step3. At file selection dialog box, select the target ASCII file, `*.PcbDoc` to import it.



There is a format to import Altium Designer as below.
[Example of `*.PcbDoc`]

```
|RECORD=Board|SELECTION=FALSE|LAYER=UNKNOWN|LOCKED=FALSE|POLYGONOUTLINE=FALSE|U
|RECORD=Board|TOPTYPE=3|TOPCONST=3.500|TOPHEIGHT=0.4mil|TOPMATERIAL=Solder Resi
|RECORD=Board|LAYER6NAME=MidLayer5|LAYER6PREV=0|LAYER6NEXT=0|LAYER6MECHENABLED=
|RECORD=Board|LAYER11NAME=Mid-Layer 10|LAYER11PREV=0|LAYER11NEXT=0|LAYER11MECHE
|RECORD=Board|LAYER16NAME=Mid-Layer 15|LAYER16PREV=0|LAYER16NEXT=0|LAYER16MECHE
|RECORD=Board|LAYER21NAME=Mid-Layer 20|LAYER21PREV=0|LAYER21NEXT=0|LAYER21MECHE
|RECORD=Board|LAYER26NAME=Mid-Layer 25|LAYER26PREV=0|LAYER26NEXT=0|LAYER26MECHE
|RECORD=Board|LAYER31NAME=Mid-Layer 30|LAYER31PREV=0|LAYER31NEXT=0|LAYER31MECHE
|RECORD=Board|LAYER36NAME=Bottom Paste|LAYER36PREV=0|LAYER36NEXT=0|LAYER36MECHE
|RECORD=Board|LAYER41NAME=InternalPlane3|LAYER41PREV=0|LAYER41NEXT=0|LAYER41MEC
|RECORD=Board|LAYER46NAME=Internal Plane 8|LAYER46PREV=0|LAYER46NEXT=0|LAYER46M
|RECORD=Board|LAYER51NAME=Internal Plane 13|LAYER51PREV=0|LAYER51NEXT=0|LAYER51
|RECORD=Board|LAYER56NAME=Keep-Out Layer|LAYER56PREV=0|LAYER56NEXT=0|LAYER56MEC
```

※The extension of Altium Protel 99 SE is same with `*.pcb`, but the format is same as Altium Designer. So, user has to import ASCII file with using 'Altium Designer' menu.

3.2. Cadence Allegro Expansion/Spectra/OrCAD Interface

Cadence does not support ASCII extraction menu itself, but users can use executable file, `extracta.exe` to get ASCII files. To use this command, users do not need license but Allegro installation environment.

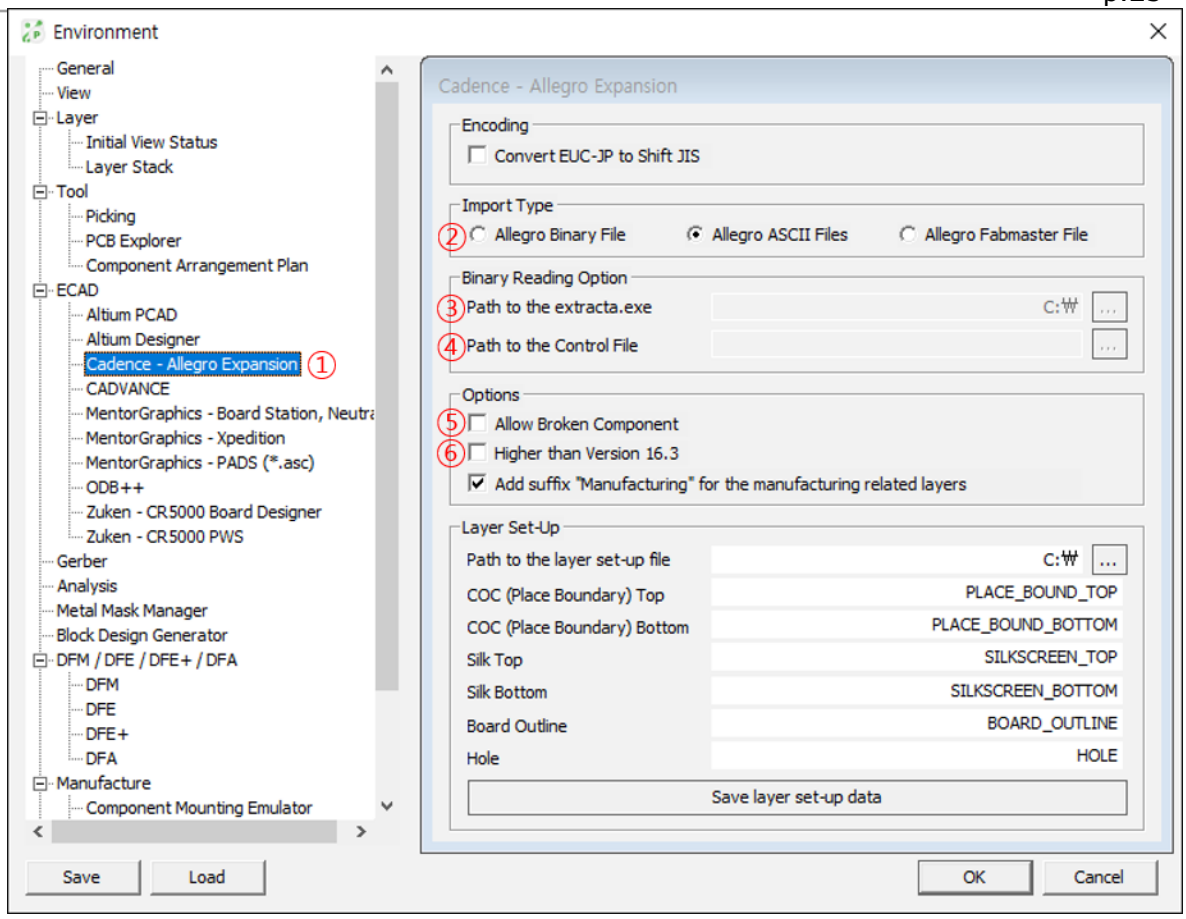
3.2.1. Cadence - Allegro Expansion

1) Direct Allegro file reading using binary file, `*.brd`.
2) Allegro file reading using ASCII files.

3.2.1.1. Direct Allegro file reading using binary file, `*.brd`.

Step1. Setup Environment for Interface

Once user sets environment for Allegro, every time when users import Allegro file in PollEx PCB, user does not need any other additional setting.



① Select menu, Setting > Environment > ECAD > Cadence – Allegro Expansion.

② Set the default reading type whether user import design from binary or ASCII file.

③ If user wants to use the way of reading binary file, set executable command file, `extracta.exe` path.
Example: `%ALLEGRO_INSTALL_DIR%\tools\pcb\bin`

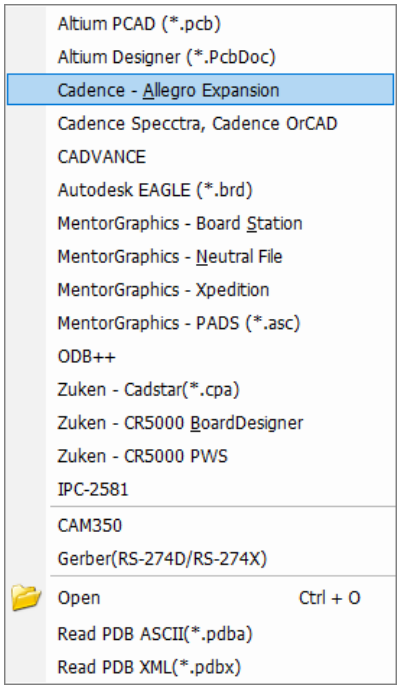
④ To use Allegro ASCII extraction command, `extracta.exe`, user need to use control file for extract ASCII file. Set the path for control file.
Example:
`C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share\AllegroExpansion_ExtractCommandFile163.txt`

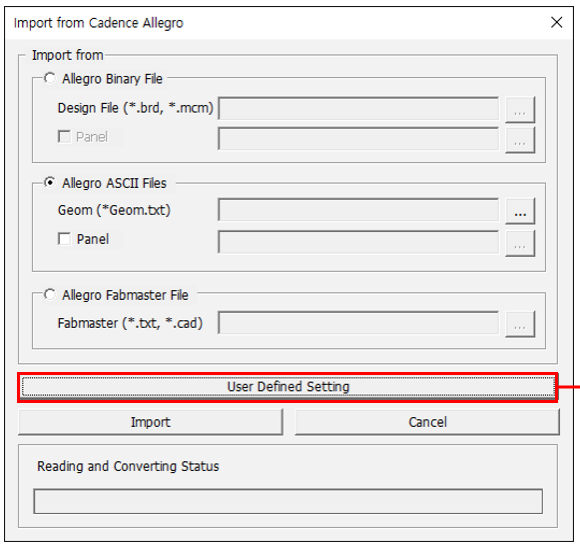
⑤ Check whether user wants to use break component or not. **Break Component** means reference components which are different than prototype in library.

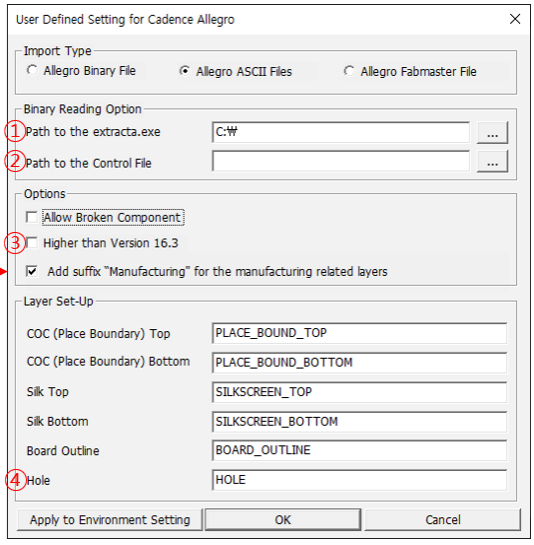
⑥ Check **Higher than Version 16.3** when user wants to read the design from Allegro version 16.3.

Step2. Allegro design reading using original binary file, `*.brd` – use one of following two ways.

File > Import ECAD > Cadence - Allegro Expansion





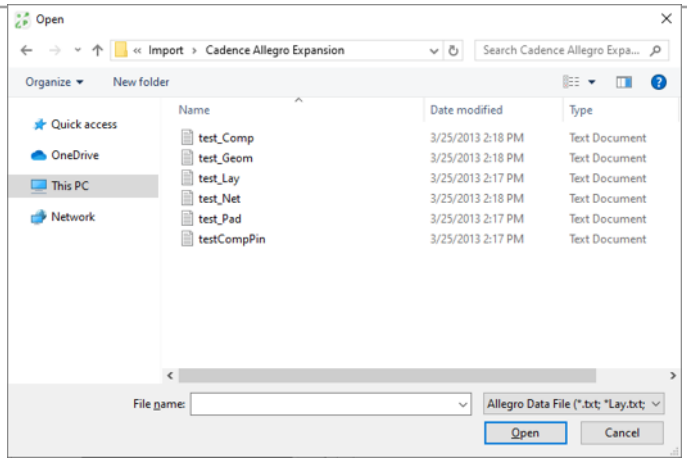


Item ① are showing the contents set on environment. At ②, select the Allegro binary file, `*.brd` and press the button menu, **Read from Binary** will start reading Allegro file. If the check box ③ is ON status, PollEx PCB Allegro reader will check Allegro version whether it is version 16.3 or not.

Hole (④): For the design file created by Allegro version 16.3, if there is another defined hole on certain layer, specify the hole layer name.

Using the environment setup, user does not need to setup Allegro reading parameters at this window.

3.2.1.2. Cadence – Allegro Expansion



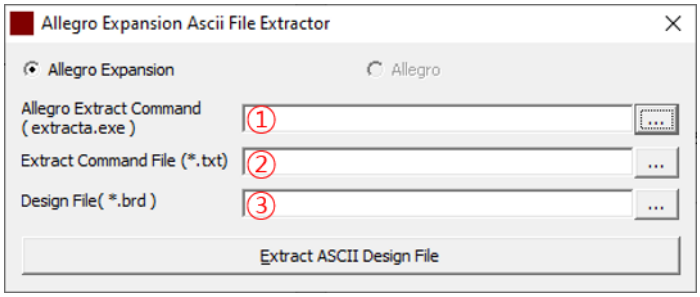
As the same with Allegro reading case, Allegro Expansion reading also left some of ASCII files. In this case, there are 6 ASCII files, `*.Comp`, `*.CompPin`, `*.Geom`, `*Lay`, `*.Net` and `*.Pad`. PollEx PCB reads these 6 files after running `extracta.exe` command.

3.2.2. Allegro file reading using ASCII files.

Step1. Extracting ASCII File
Following two windows guide users to extract ASCII file from Allegro binary design file, `*.brd`.

3.2.2.1. Allegro Expansion Reading Case.

Use the Allegro ASCII file extraction command, AllegroExpansionASCIIExtractor.exe in the path, C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share.



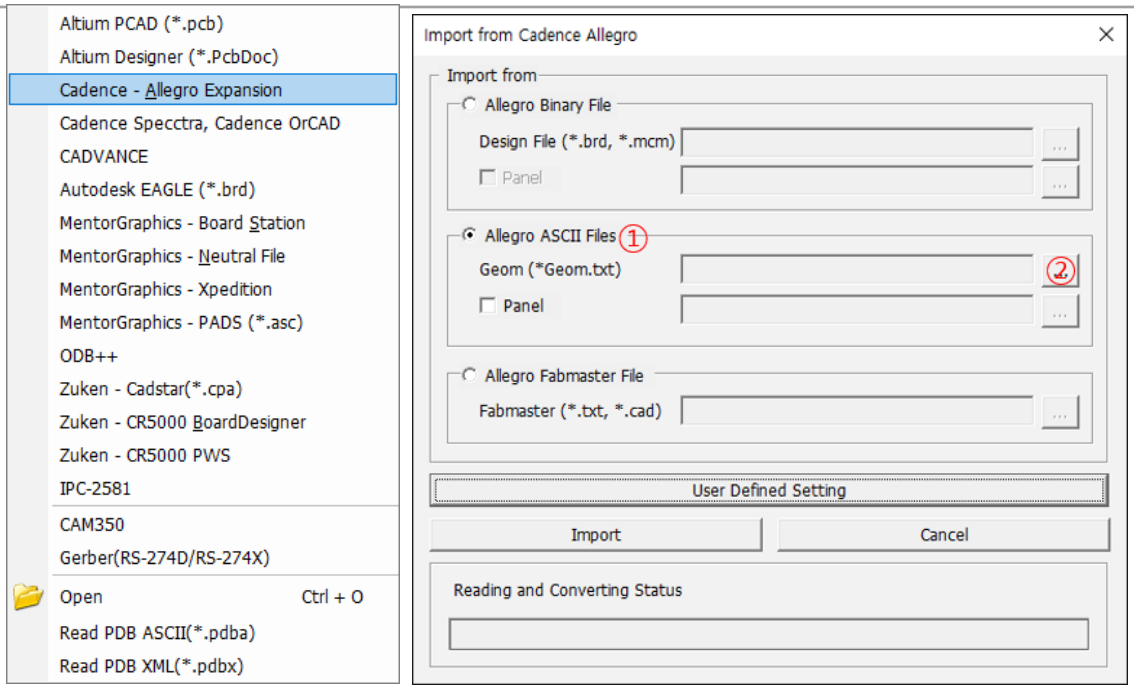
At ①, specify the Allegro ASCII extraction command file, `extracta.exe` path.

At ②, give the control file, AllegroExpansion_ExtractCommandFile.txt path under C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share.

At ③, select target Allegro design file.

Upon pressing the button, Extract ASCII Design File will make 6 different ASCII files.

Step2. Import Allegro using ASCII file.
Use one of following two menus to import Allegro design.
File > Import ECAD > Cadence – Allegro Expansion



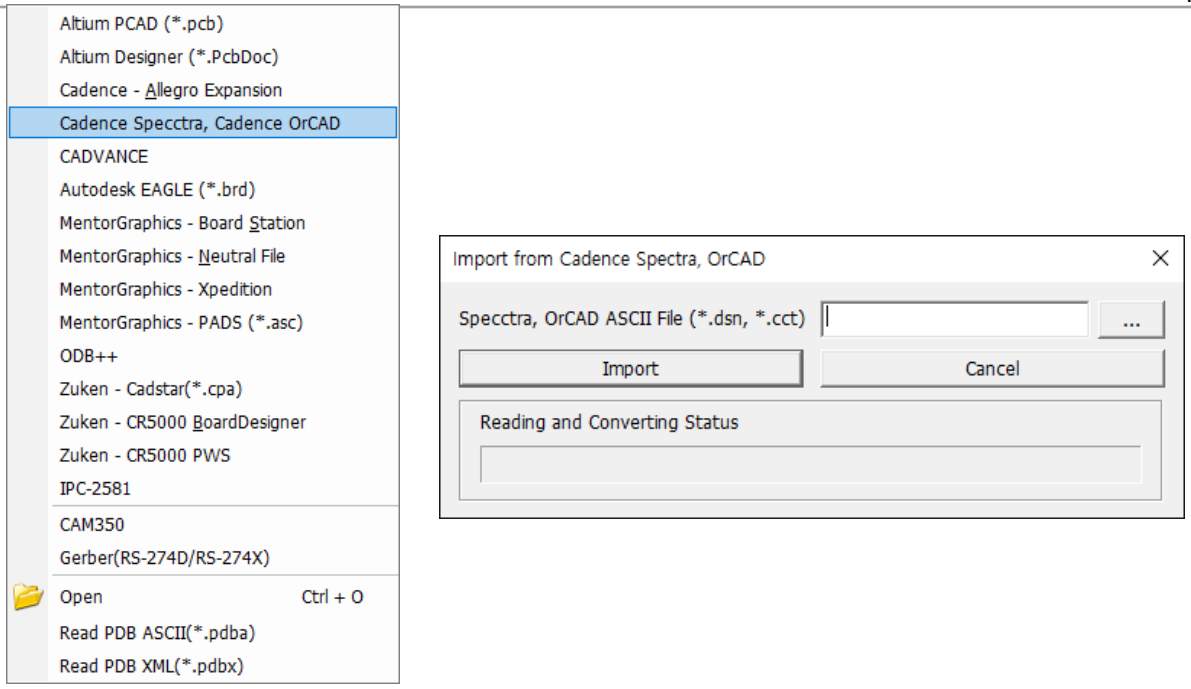
At ①, to read Allegro design with ASCII file, the reading type check button should be **Read from ASCII File**. User can set this setting in environment.

Using the button ② for Allegro Expansion reading, users can select ASCII files. Finally, upon pressing the button, **Read from ASCII**, import selected ASCII files and convert them to PollEx PCB design job file, `*.PDBB`.

3.2.3. Cadence - Spectra/OrCAD

The file extension of Cadence Spectra is `*.dsn`. Schematic file of Cadence OrCAD has also same file extension, so be cautious when user selects file.

Step1. Extract ASCII file, *.dsn from Cadence Spectra.
Step2. Use the menu, **File > Import ECAD > Cadence Spectra/Cadence OrCAD**.

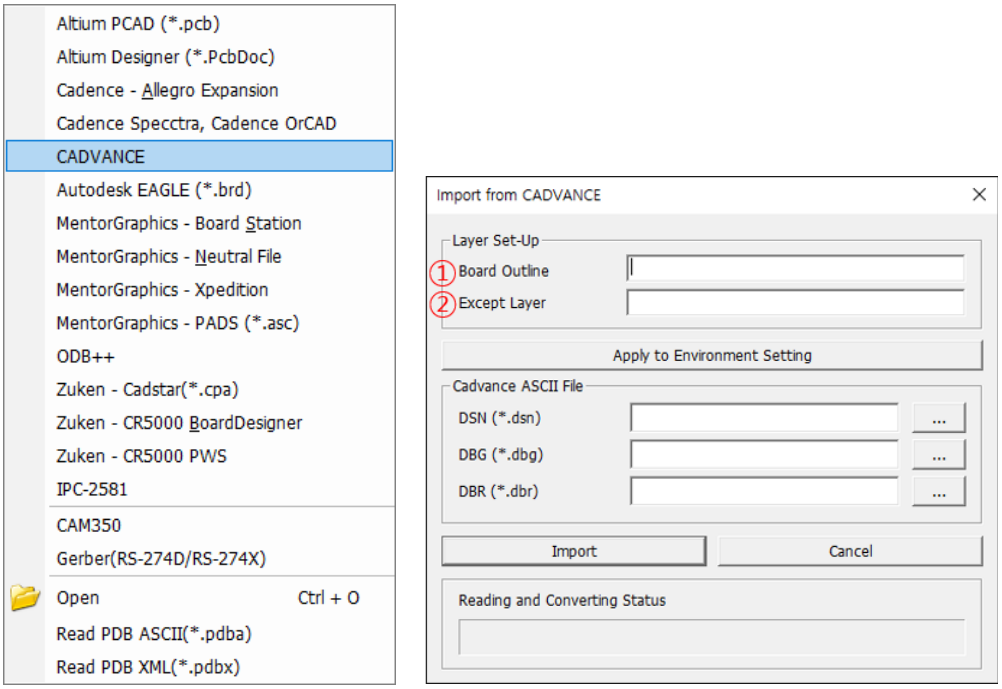


Another way of reading Spectra file is using utility program of Allegro. Allegro utility program converts Spectra file to Allegro design file, `*.brd` and uses Allegro reader in PollEx PCB.

3.2.4. CADVANCE Interface

PollEx PCB supports CADVANCE files such as `*.dsn`, `*.dbg` and `*.dbr` files.

Step1. Extract ASCII file, `*.dsn`,`*.dbg`,`*.dbr` from CADVANCE.
Step2. Use the menu, **File > Import ECAD > CADVANCE**.

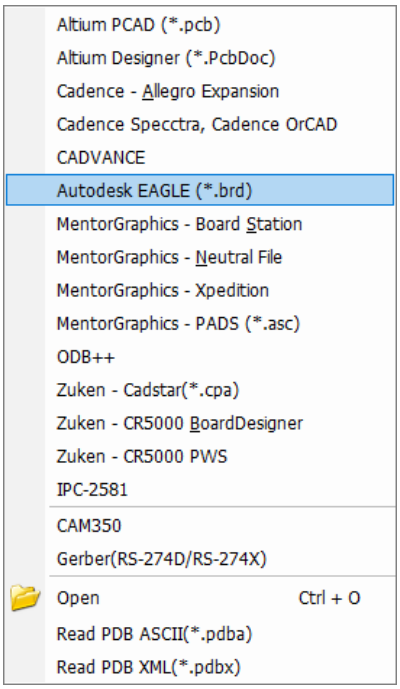


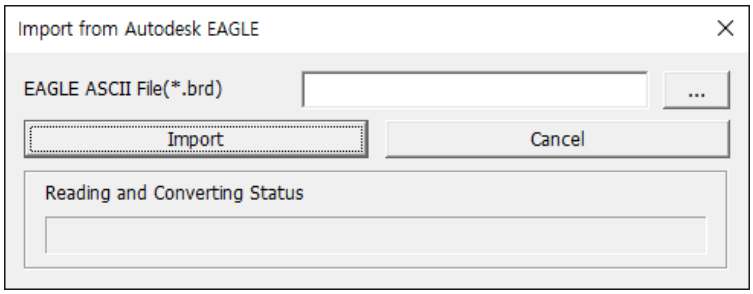
① If there is a specific layer for board outline, specify the layer name. This layer will be transferred to layer number 21 in PDB structure.
② In case of CADVANCE Interface, it might be big data because it brings all layer's information from CADVANCE ASCII. So, it can be excepted the specific layer.

3.2.5. Autodesk EAGLE Interface

PollEx PCB supports EAGLE CAD file such as `*.brd` file.

Step1. Extract ASCII file, `*.brd` from Autodesk EAGLE.
Step2. Use the menu, **File > Import ECAD > Autodesk**.





3.3. Mentor Graphics Interface

Mentor Graphics is releasing several different ECAD tools, PADS PowerPCB, Board Station and Expedition.

3.3.1. Mentor Graphics - Board Station

PollEx PCB's Mentor Graphics - Board Station reader use following 5 ASCII files.

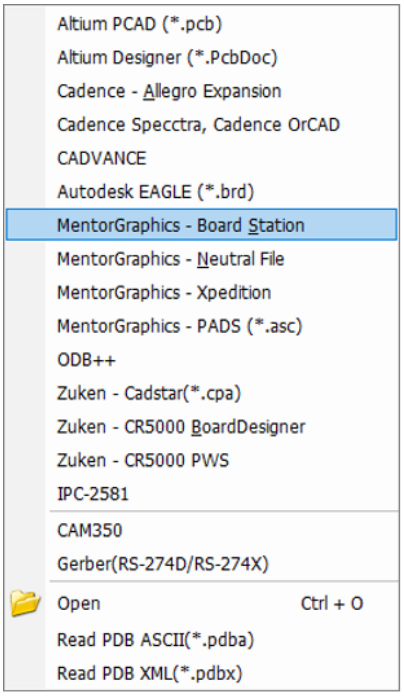
File	Example
comp.com_XXX	comps.comp_256
net.net_XXX	nets.net_123
traces.traces_XXX	traces.traces_123
tech.tech_XXX	Tech.tech_123
geometry file	`*.geom`

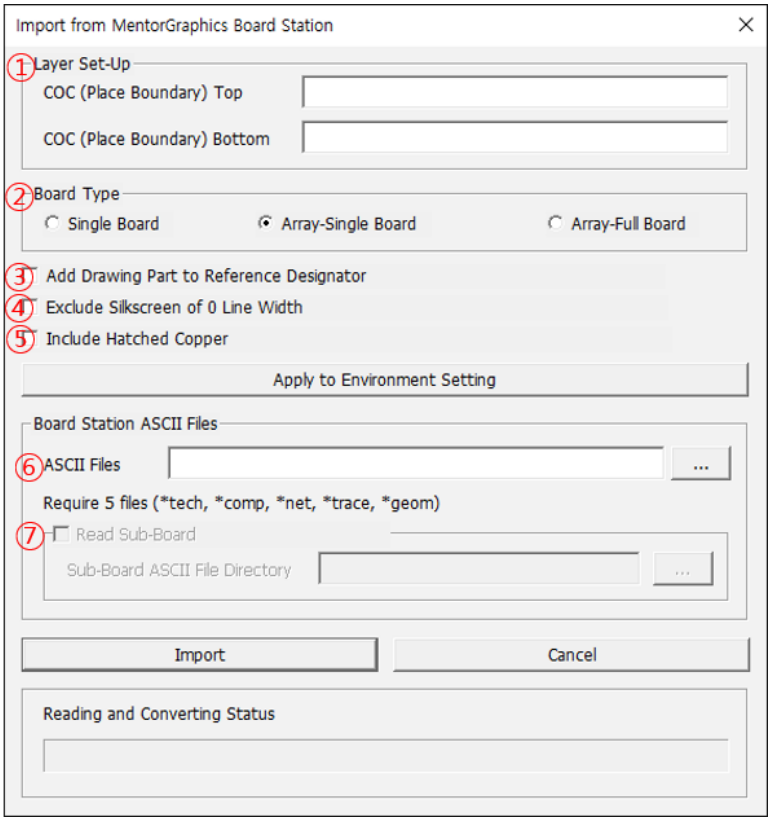
In Board Station working folder, there are 4 files except Geometry file. Among many files, select a file having header, comp, net, and trace and tech files with the highest revision number. It means they are latest files. However, user does not need `tech.tech_`XXX file, if user did not use blind or buried via.

Step1. Extraction Geometry files in Board Station.

1. Open Job file and launch librarian.
2. Use the menu, **File > Save > Save ASCII Geometries**.
3. Select **All Geometries** and **One File** and save file in certain path with extension, `*.geom`.

Step2. Reading Mentor Graphics Board Station ASCII in PollEx PCB.
Use the menu, **File > Import ECAD > Mentor Graphics - Board Station**.





① Specify the artwork layer name to recognize as COC Top and Bottom.
② Select reading board type.
- **Single Board**: Use this option for reading single board.
- **Array-Single Board**: Use this option for reading array board contour and single board.
- **Array-Full Board**: Use this option for reading array board contour and full single board.

③ Add drawing part to reference designator.
④ **Exclude Silkscreen of 0 Line Width:** Excludes silkscreen having a line width of zero.
⑤ Check this option if the hatched copper is used in the design.
⑥ At any column if user selects one among 5 ASCII files, others are automatically assigned to each folder column. At this time, if there are multiple files having same name but different version, PollEx PCB will automatically select the latest version.
⑦ Check this option when users use generic parts in array board and want them to be part of sub board.

3.3.2. Mentor Graphics - Neutral File

PollEx PCB also can read Board Station's neutral file and followings are necessary ASCII files for importing into PollEx PCB.

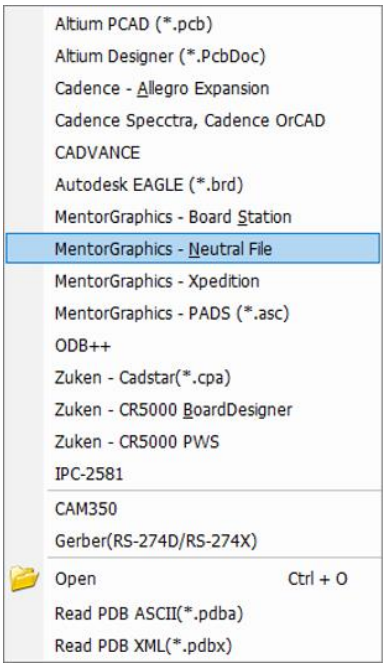
File	Example

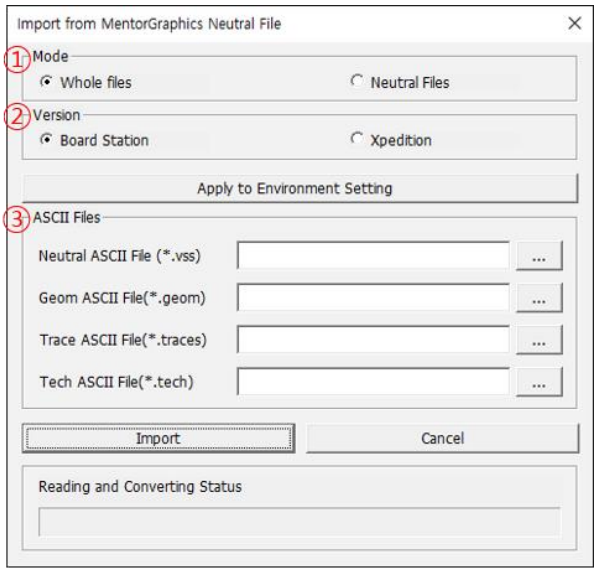
neutral_file	neutral.vss
traces.traces_XXX	traces.traces_123
tech.tech_XXX	tech.tech_123
geometry file	*.geom

If user did not use blind/buried via, `tech.tech_XXX` file is not needed.

Step1. Extract Geom file in Board Station
1. Open jog file and launch librarian.
2. Use the menu, **File > Save > Save ASCII Geometries**.
3. Select **All Geometries** and **One File.** Then, save file with extension name `*.geom` into a certain folder.

Step2. ASCII importing in PollEx PCB.
Use the menu, **File > Import ECAD > Mentor Graphics - Neutral File**.





① Choose the type of ASCII file. **Neutral Files** will read only component placement and netlist information. There is no routing information. On the other hand, **Whole Files** will read all PCB related information. When selected **Whole Files**, PollEx PCB will read 4 files, `tech.tech***`, `neutral`, `ASCII_GEOM` and `trace.trace***`.
② Choose the version **Mentor Board Station** or **Mentor Xpedition**.
③ User can select necessary files individually.

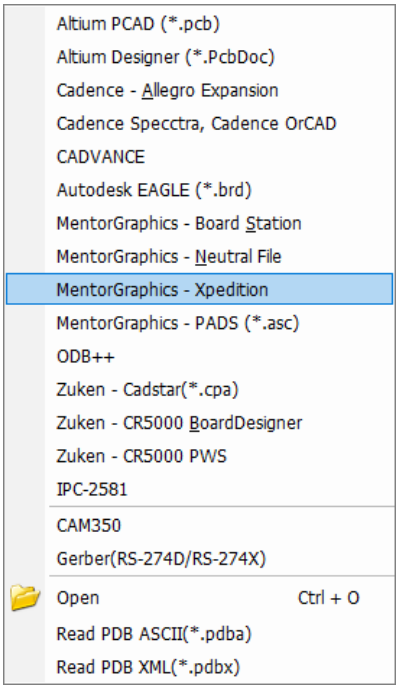
3.3.3. Mentor Graphics - Xpedition

PollEx PCB read Mentor Graphics Xpedition's 6 ASCII files. Following table shows all necessary files and their information.

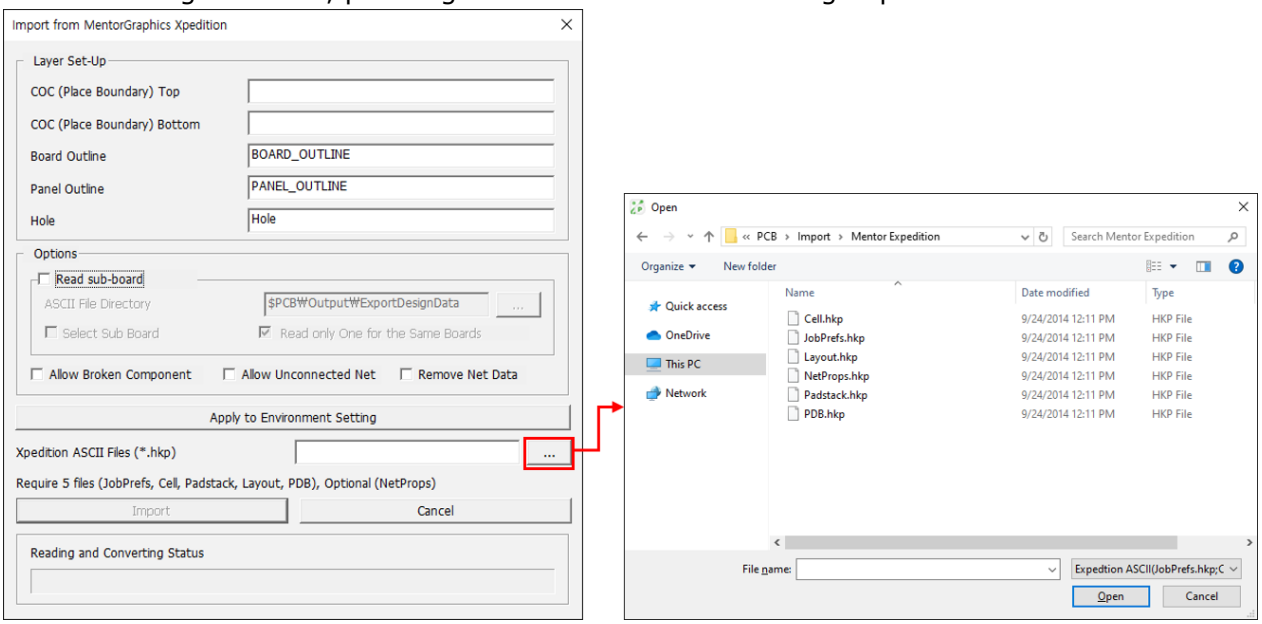
File Name	Description
`Cell.hkp`	Component placement information
`JobPrefs.hkp`	Layer information
`Layout.hkp`	Routing information
`NetProps.hkp`	Net information
`Padstack.hkp`	Padstack information
`PDB.hkp`	Part library information

Step1. Extract ASCII file from Mentor Graphics Xpedition.

Step2. Use the menu, **File > Mentor Graphics – Xpedition**.



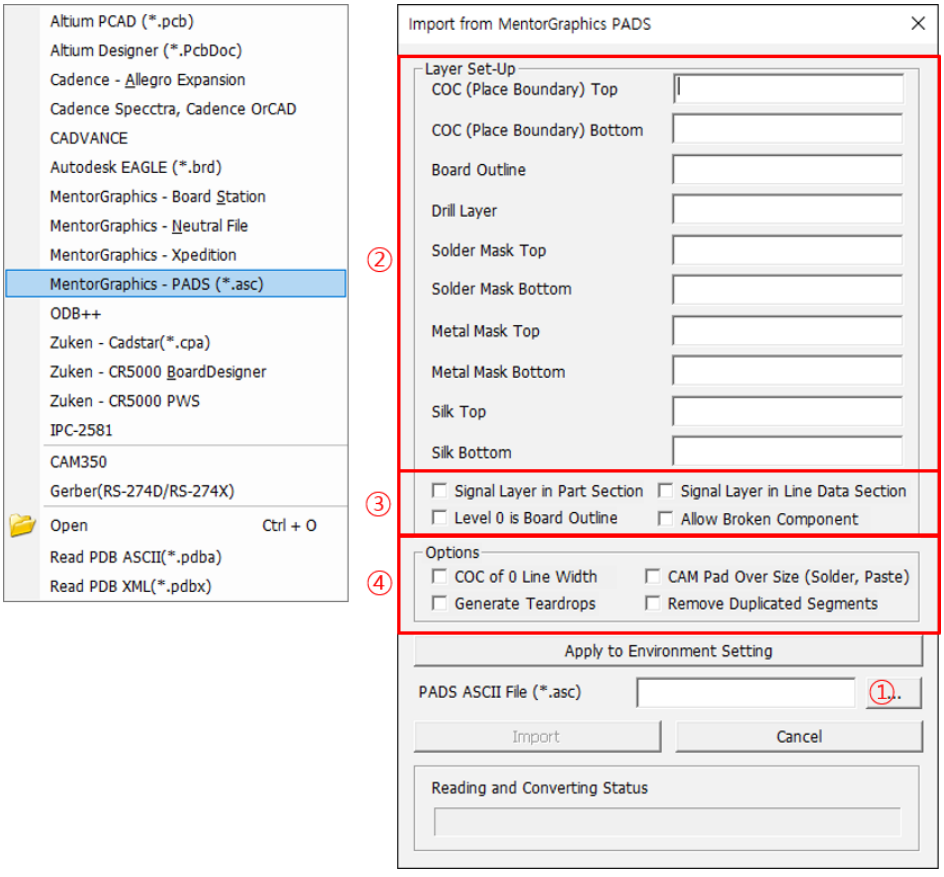
After selecting all 6 files, pressing OK button will start reading Expedition into PollEx PCB.



3.3.4. Mentor Graphics - PADS

Users can export Mentor Graphics PADS design to ASCII file, `*.asc`. Depending on ASCII version of PowerPCB, they might be different, but PollEx PCB will support every version of them.

Step1. Extract ASCII file from Mentor Graphics PADS.
Step2. Use the menu, **File > Import ECAD > Mentor Graphics – PADS**.



① After selecting menu, **PADS ASCII File** (`*.asc`), press the button menu to read from PADS ASCII file.

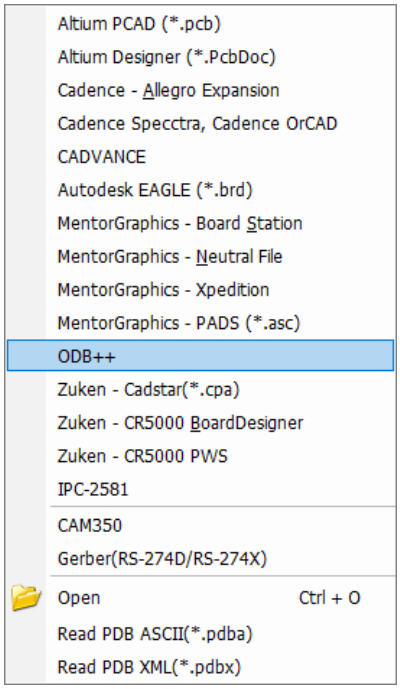
② **Layer Setting** is an optional. Specify artwork layer name per each menu.
- COC Top/bottom: PollEx DFM will use these layers' data for measure base.
- Board Outline: If there is the specific layer for board contour, give that layer name. This layer will be transferred to layer number 21 in PDB structure.
- Drill Layer: If there is the specific layer for drill, give that layer name. This layer will be transferred to layer number 22 in PDB structure.

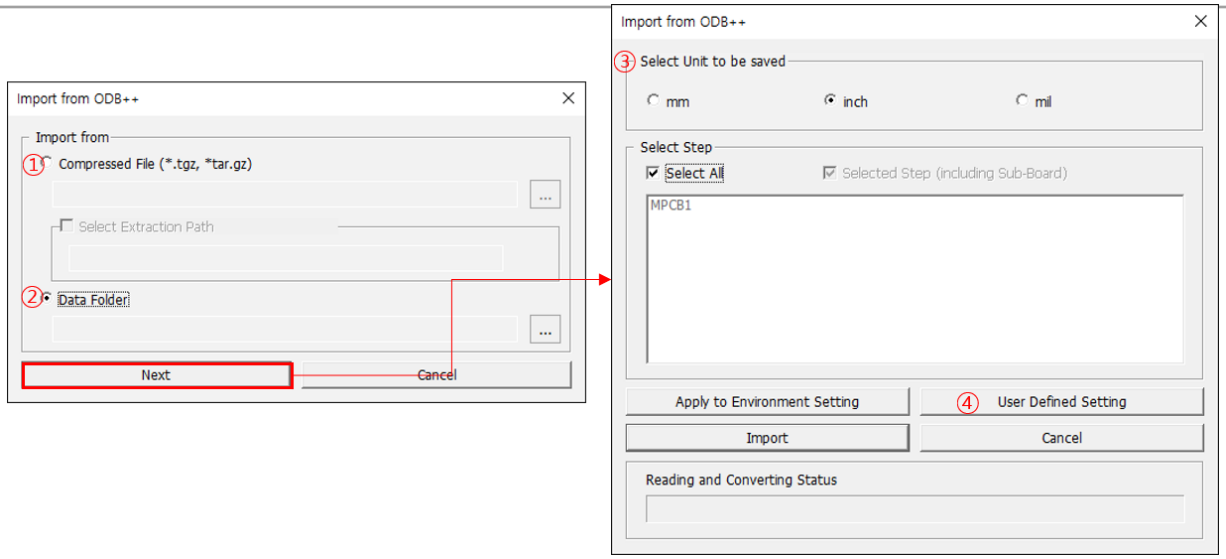
③ **Signal Layer in Part Section**: In footprint definition, check this option if object layer is signal layer.
Signal Layer in Line Data Section: In board figure definition, check this option if object layer is signal.
Level 0 is Board Outline: Check this option if layer level 0 is board contour layer.
Allow Broken Component: Check this option if Broken Component is used.

④ **COC of 0 Line Width**: Check this option if line width of COC as 0.
CAM Pad Over Size (Solder, Paste): Check this option if solder mask definition is recorded in CAM.
Generate Teardrops: This option is used automatically generated teardrop shape at PAD and Via.
Remove Duplicated Segments: Check this option to remove duplicated segments.

3.4. ODB++

ODB++ is ASCII format of Mentor Graphics to complement the weakness of GERBER format. Thus, it has all intelligent design information. PollEx PCB also supports this format. To import ODB++ file, use the following menu, **File > Import ECAD > ODB++**.



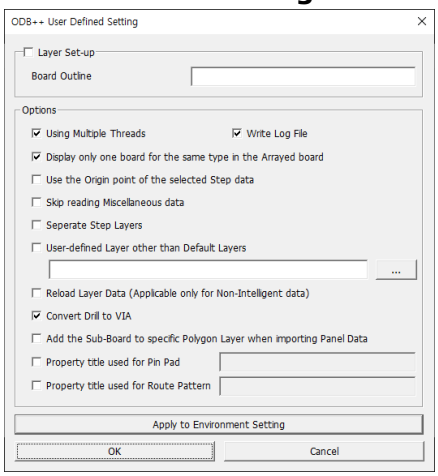


① **Compressed File:** Select ODB++ compressed file. Also, define additional option about uncompressing path. The folder is created in the uncompressing path.

② **Data Folder:** If the ODB++ file system exists as a folder structure, select the top level folder in hierarchical folder structure. Select top folder in folder searching dialog window.

③ **Select Unit to be Saved:** Specify the unit of PDBB, not the unit used in ODB++ design.

④ **User Defined Setting:** Enable user to specify parameters for data importing options.



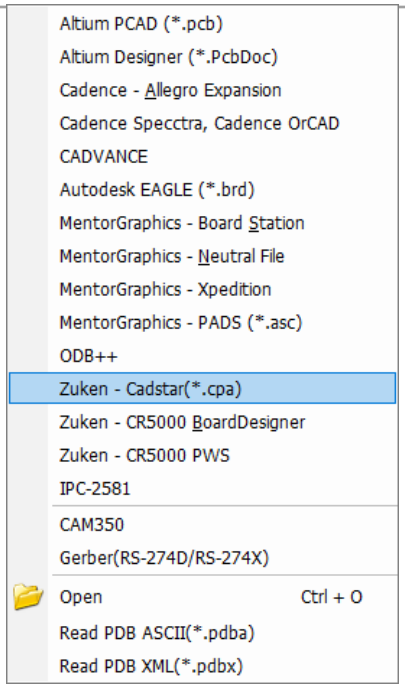
3.5. Zuken Interface

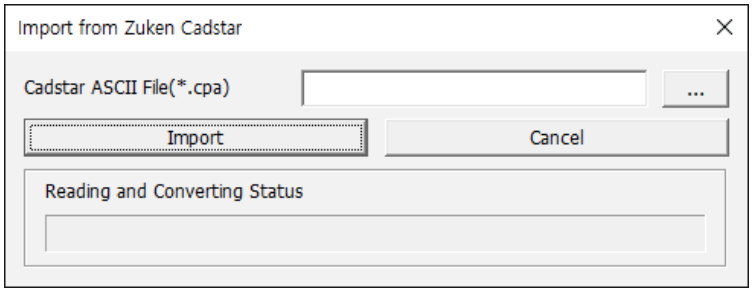
PollEx PCB supports various Zuken's CAD design files, Cadstar, Board Designer and PWS.

3.5.1.1. Zuken – Cadstar (`*.cpa`)

Step1. Extract ASCII file from Zuken Cadstar.

Step2. Use the menu, **File > Import ECAD > Zuken - Cadstar(*.cpa).**





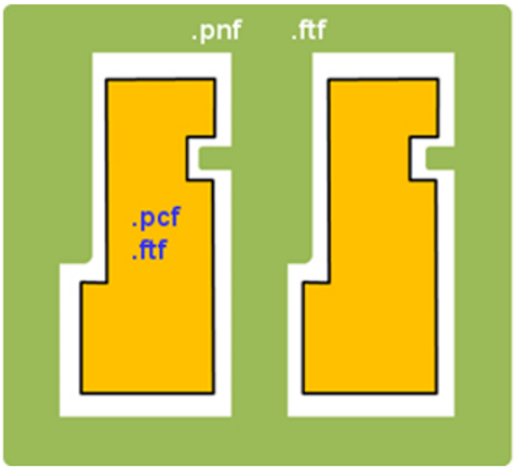
Select *.cpa and pressing OK button start reading Zuken CADSTAR design.

3.5.1.2. Zuken - CR5000 Board Designer

PollEx PCB can read Zuken BD (Board Designer) ASCII file. Upon using the utility, user can extract ASCII file from Zuken BD's binary design, `*.pcb`.

Step1. ASCII files extraction using utility command, `BDExtractor.exe`.

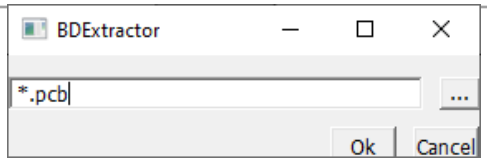
PollEx PCB supports two types of board types, single and arrayed board to read Zuken Board Designer. Array board file, `*.pnf` should have single boards information in it and at same time, single board files, `*.pcf` should also exist at certain folder.



Type	ASCII File	
Single Board	*.pcf, *.ftf	
Array Board	*.pcf, *.ftf	*.pnf, *.ftf

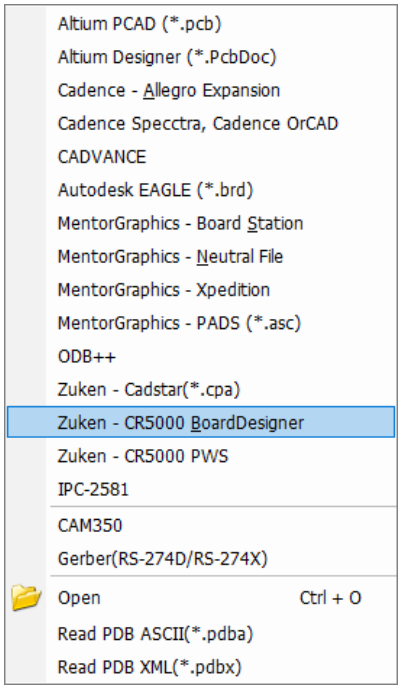
To get ASCII file from Zuken BD, use the utility command, `BDExtractor.exe`.

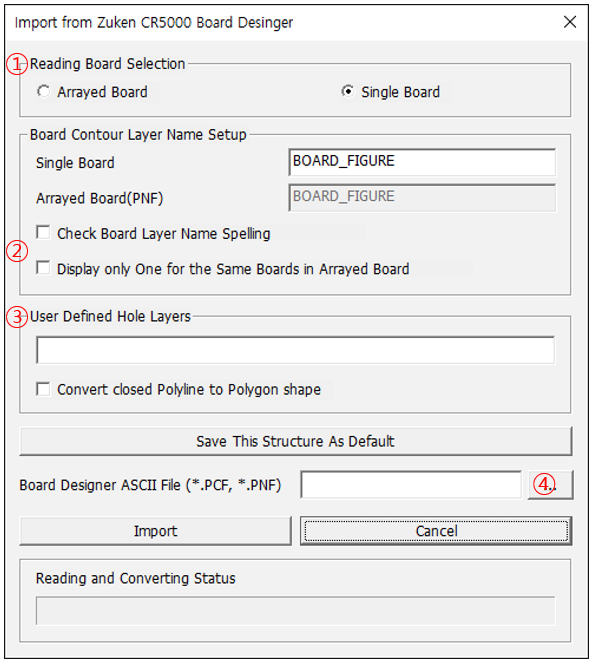
Using this command, user can extract single and array board. File location is under `C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share\BDExtractor.exe`.



After specifying design file, *.pcb, press the OK button to start ASCII file extraction.

Step2. Importing design into PollEx PCB using ASCII files.
Use the menu, File > Import ECAD > Zuken - CR5000 Board Designer.





① Select the board type between Arrayed Board and Single Board.
② For the single and arrayed board, user can define the layer name of board contour layer. Then, user can also define the rule to read as many as number of single boards or just one for same type board during arrayed board reading case.
③ Specify the layer name in Board Designer to be used with hole data layer in PDB.
④ PollEx PCB read 2 ASCII files, `*.pcf` and `*.ftf`, but it is enough to specify with `*.pcf`. PollEx PCB automatically find `*.ftf` file in the same folder. For reading arrayed board, another two files, `*.pnf` and `*.ftf`, are necessary.

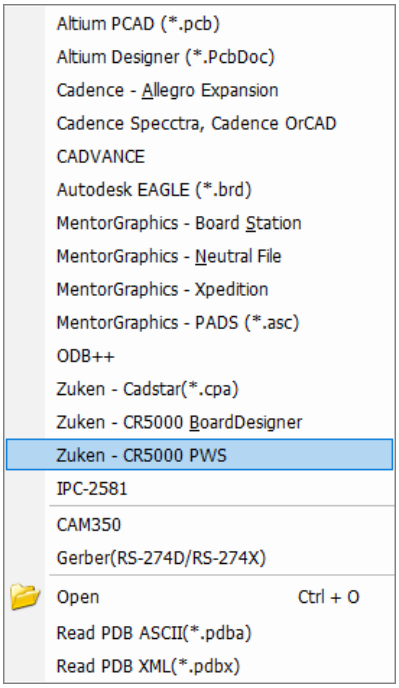
3.5.1.3. Zuken - CR5000 PWS

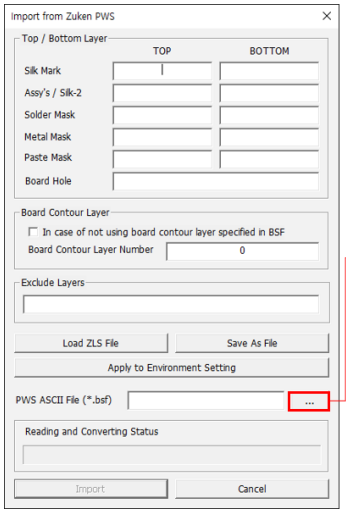
PollEx PCB supports two types of reading, artwork and wiring modes for Zuken PWS. Artwork mode means that all objects in design have no intelligent information like net name. All routing patterns exist on physical layers, but they don't have net information, so they will be transferred to just graphic data. In this case, after reading design with artwork mode, user cannot use these designs for nets related function or for electrical analysis.

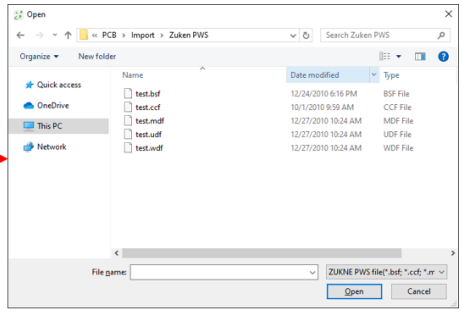
All needed ASCII files are following 5 files.

`*.BSF`	Board specification information file.
`*.CCF`	Net information file.
`*.MDF`	Part information file.
`*.UDF`	Component placement and board graphic information file.
`*.WDF`	Routing pattern information file.

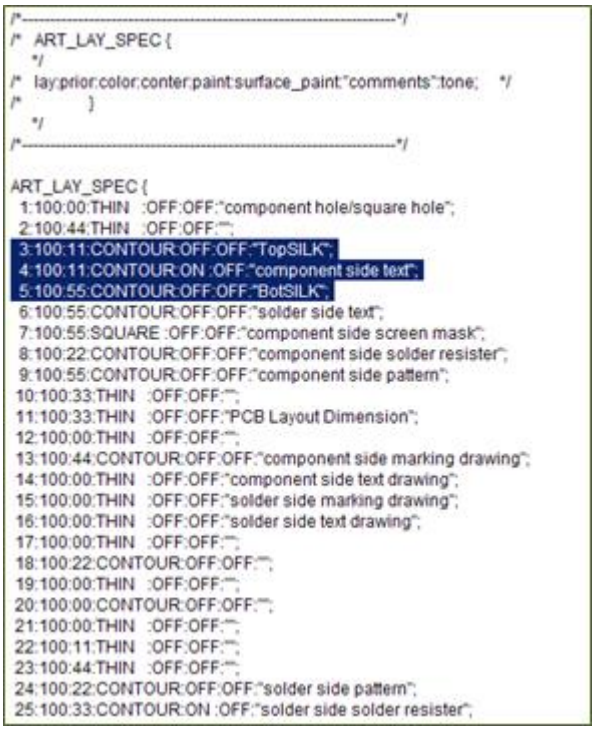
Step1. Extract ASCII file from Zuken CR5000 PWS.
Step2. Use the menu, **File > Import ECAD > Zuken – CR5000 PWS.**







Among the 5 files, select any one of them and PollEx PCB can detect all other files and automatically read design.

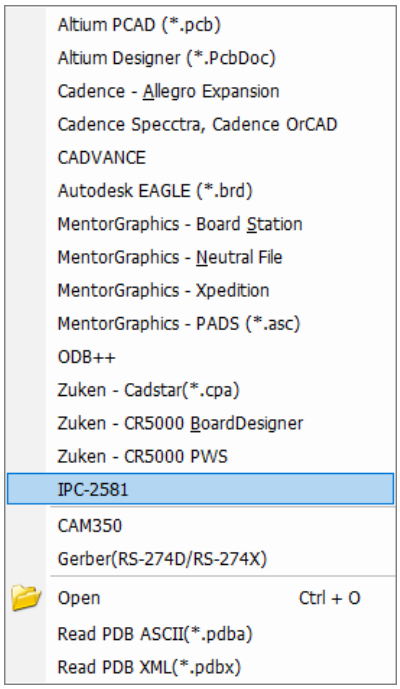


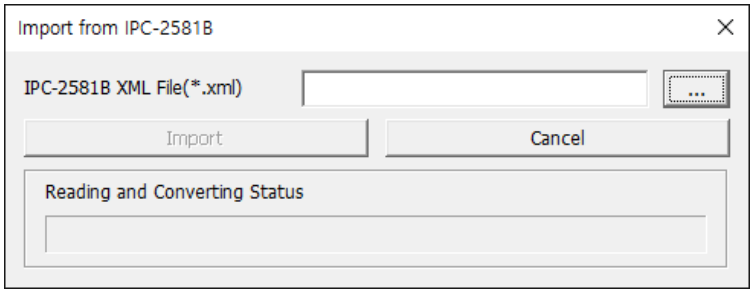
```
/*-------------------------------------------------------------------*/
/*  ART_LAY_SPEC {
   */
/*  lay:prior:color:conter:paint:surface_paint:"comments":tone;    */
/*          }
   */
/*-------------------------------------------------------------------*/

ART_LAY_SPEC {
 1:100:00:THIN  :OFF:OFF:"component hole/square hole";
 2:100:44:THIN  :OFF:OFF:"";
 3:100:11:CONTOUR:OFF:OFF:"TopSILK";
 4:100:11:CONTOUR:ON :OFF:"component side text";
 5:100:55:CONTOUR:OFF:OFF:"BotSILK";
 6:100:55:CONTOUR:OFF:OFF:"solder side text";
 7:100:55:SQUARE :OFF:OFF:"component side screen mask";
 8:100:22:CONTOUR:OFF:OFF:"component side solder resister";
 9:100:55:CONTOUR:OFF:OFF:"component side pattern";
10:100:33:THIN  :OFF:OFF:"";
11:100:33:THIN  :OFF:OFF:"PCB Layout Dimension";
12:100:00:THIN  :OFF:OFF:"";
13:100:44:CONTOUR:OFF:OFF:"component side marking drawing";
14:100:00:THIN  :OFF:OFF:"component side text drawing";
15:100:00:THIN  :OFF:OFF:"solder side marking drawing";
16:100:00:THIN  :OFF:OFF:"solder side text drawing";
17:100:00:THIN  :OFF:OFF:"";
18:100:22:CONTOUR:OFF:OFF:"";
19:100:00:THIN  :OFF:OFF:"";
20:100:00:CONTOUR:OFF:OFF:"";
21:100:00:THIN  :OFF:OFF:"";
22:100:11:THIN  :OFF:OFF:"";
23:100:44:THIN  :OFF:OFF:"";
24:100:22:CONTOUR:OFF:OFF:"solder side pattern";
25:100:33:CONTOUR:ON :OFF:"solder side solder resister";
```

To define usage of artwork layers in PWS, it is preferred to define all top/bottom corresponding layers. Depending on users, they are using different layer mapping tables in BSF. These layers mapping status can be saved into file, `*.zls` and re-use it for the next reading.

3.6. IPC-2581 Interface

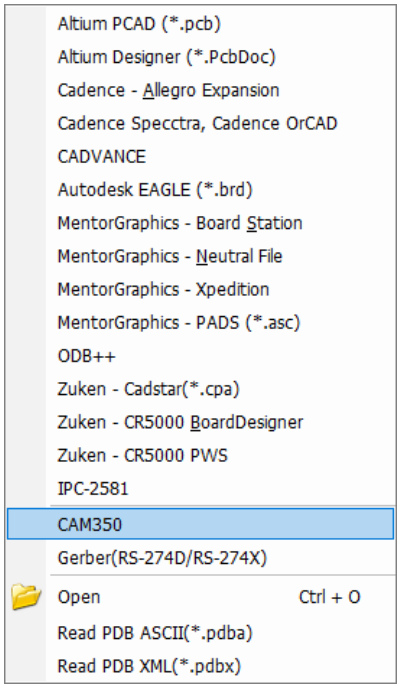
PollEx PCB supports IPC-2581 file such as `*.cvg` file.

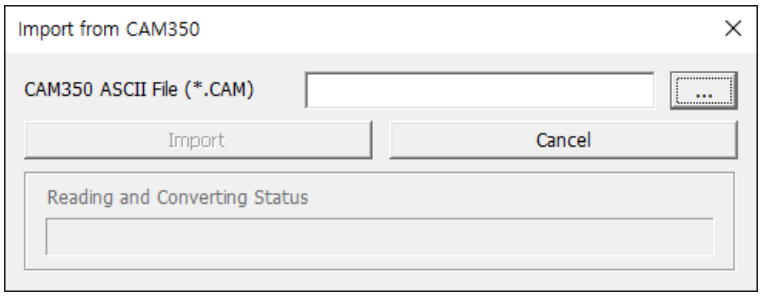




3.7. CAM 350

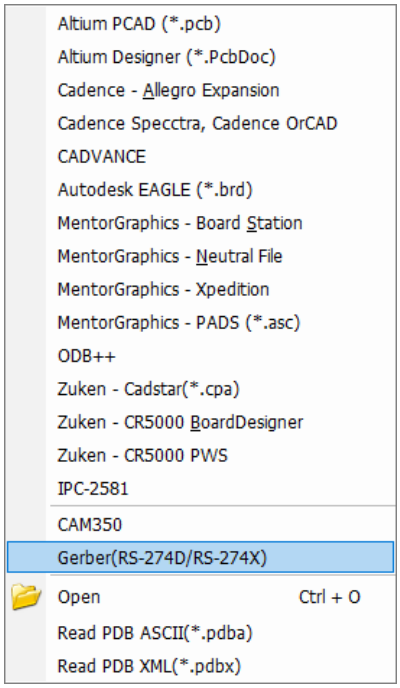
PollEx PCB supports CAM350 file such as `*.CAM` file.

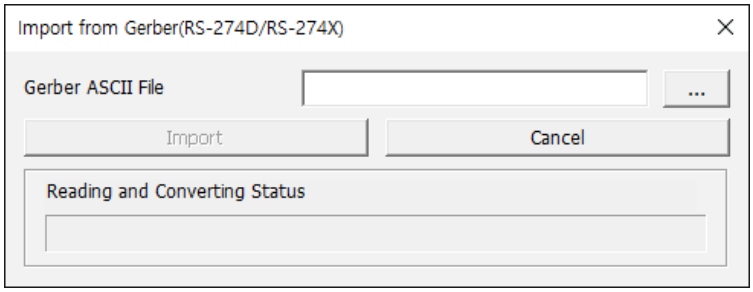




3.8. Gerber Data Interface

PollEx PCB supports four types of GERBER formats, 274X, 274D, Drill and Square Hole.
When you import Gerber Data, PollEx PCB analyze the file format internally and separate to 274X, 274D, Drill file, Square Hole and Aperture.
In case of 274D, there are necessary both of Gerber data and Aperture file.
If there are multiple aperture files, PollEx PCB make to one aperture data based on D-Code.
Use the following menu, **File > Import ECAD > Gerber(RS-274D/RS-274X).**



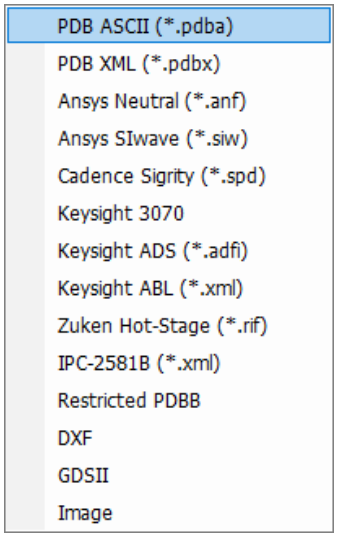


4. Export To

4.1. PollEx ASCII Interface

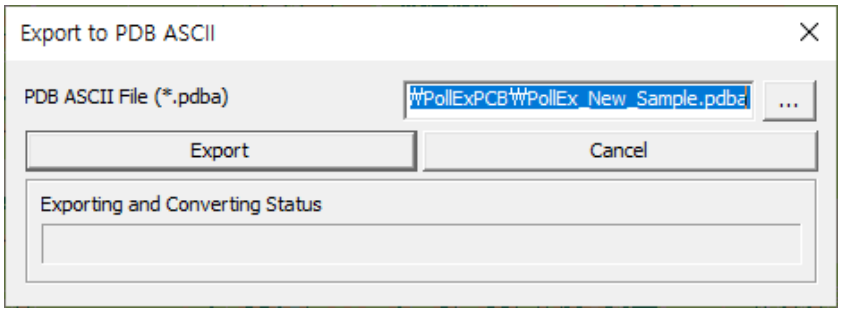
PDBB file is PollEx PCB's binary design file including all geometries and entities necessary to describe whole PCB design. In addition, PollEx PCB provides same ASCII file structure, `*.pdba`. This is ASCII version of PDBA file.

Step1. Exporting design to ASCII file, *.PDBA in PollEx PCB.
Use the menu, **File > Export To > PDB ASCII (`*.pdba`)**.



After using above menu, at file saving dialog box, specify the file name and path to export into ASCII file.

Step2. Reading ASCII file, `*.PDBA` in PollEx PCB.

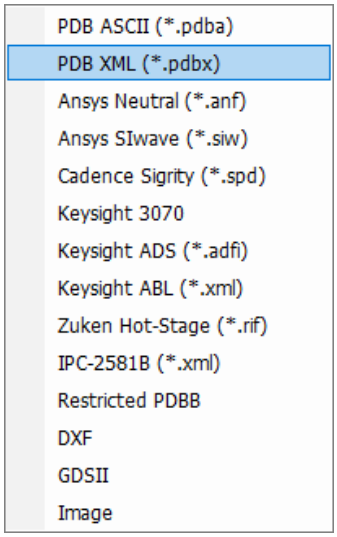


Select the file in dialog window and pressing OK button will start reading ASCII file, `*.PDBA` into PollEx PCB.

4.2. PDB XML(*.pdbx)

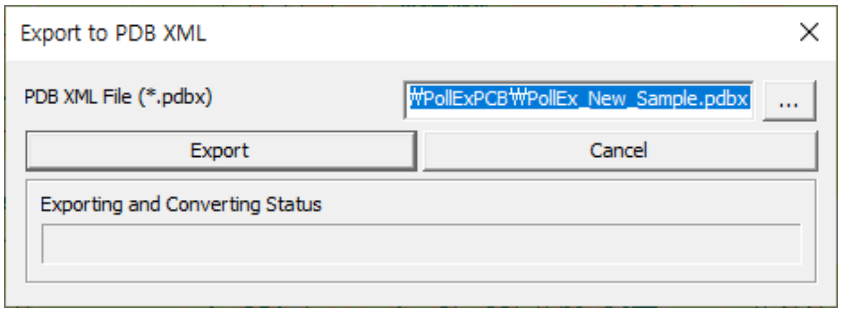
Step1. Exporting design to XML file, `*.PDBX` in PollEx PCB.

Use the menu, **File > Export To > PDB XML (`*.pdbx`).**



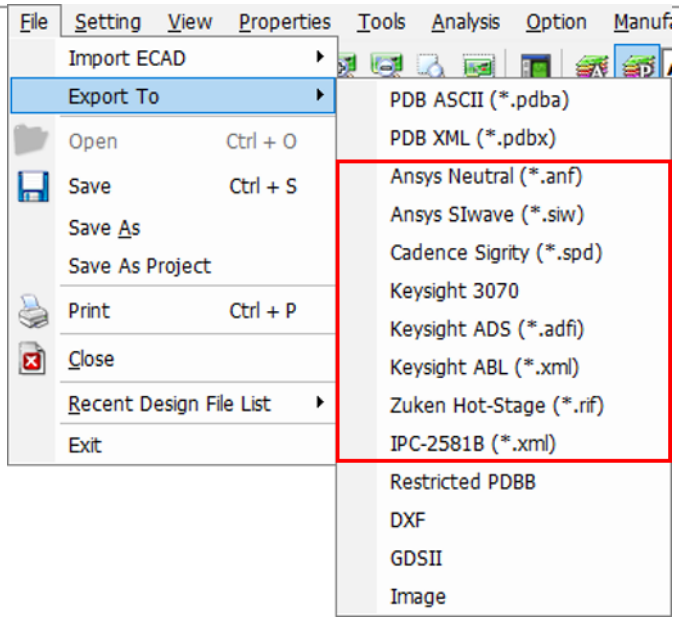
After using above menu, at file saving dialog box, specify the file name and path to export into XML file.

Step2. Reading XML file, `*.PDBX` in PollEx PCB.



4.3. Export Design to EDA vendor's Formats

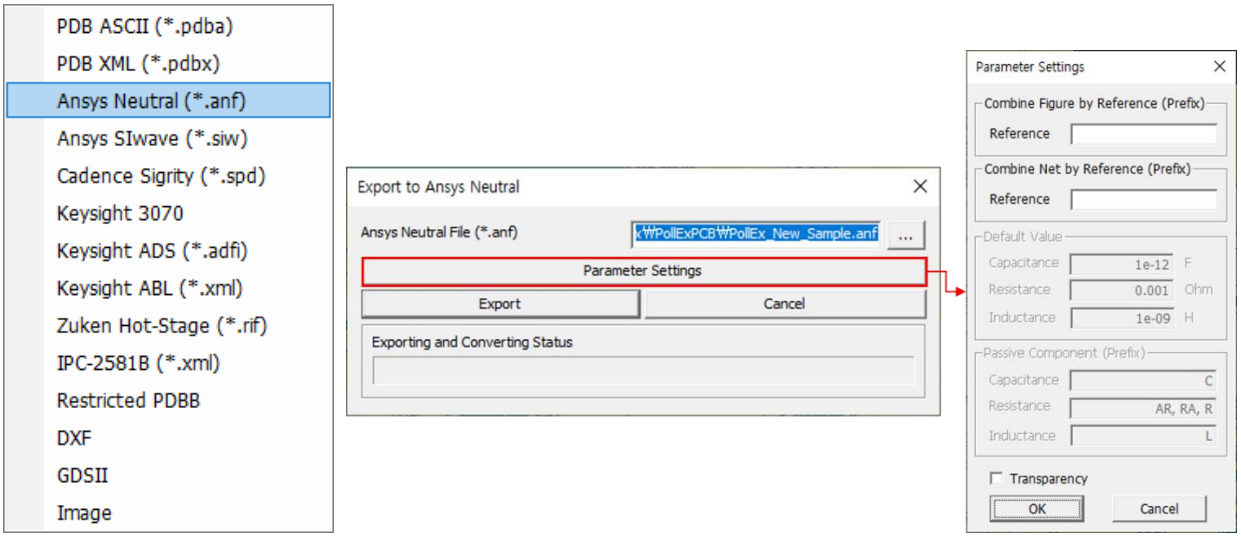
PollEx PCB supports exporting to other EDA vendors' format. Use the menus under command, **PollEx PCB > File > Export To**



PollEx PCB can export 8 different types of EDA vendors. There are Ansys Neutral File, Ansys SIWave File, Cadence Sigrity File, Keysight 3070, Keysight ADS File, Keysight ABL File(XML), Zuken Hostage, IPC-2581B.

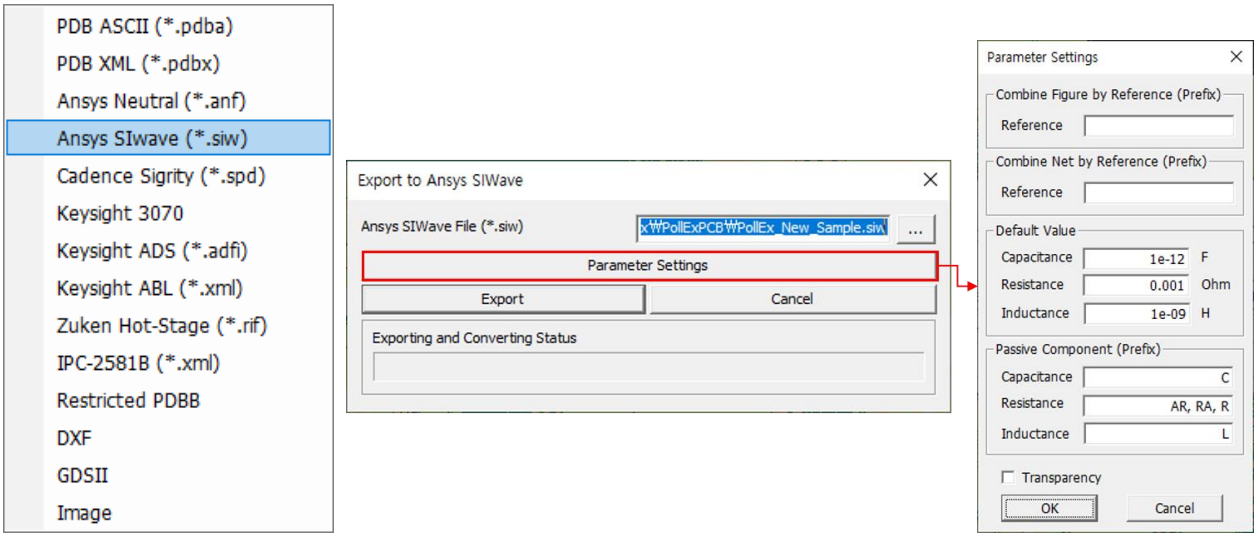
4.3.1. Ansys Neutral (*.anf)

Using this menu, user can export file to be used in Ansys Neutral. To do this work, use the menu, **File > Export To> Ansys Neutral (*.anf).**



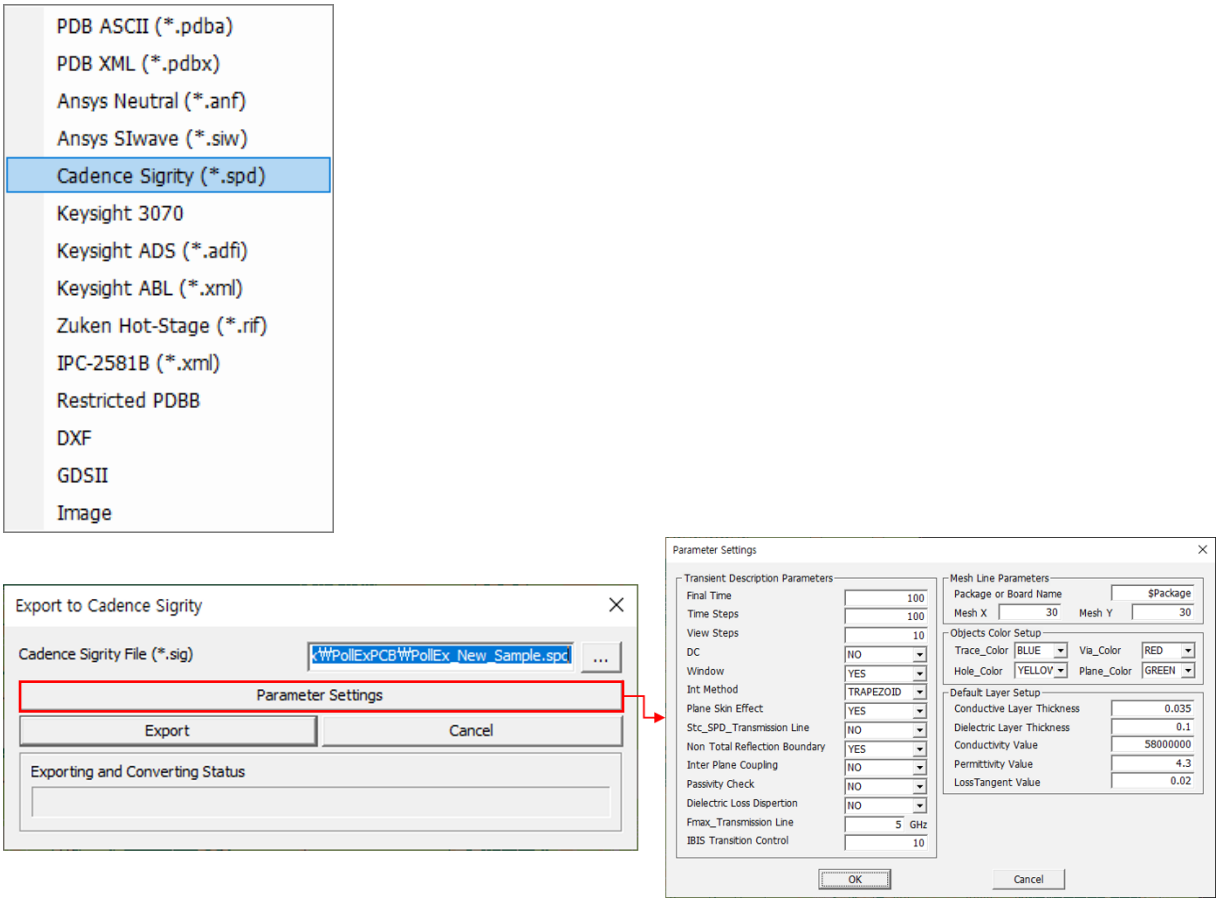
4.3.2. Ansys SIwave (*.siw)

Using this menu, user can export file to be used in Ansys SIWave. To do this work, use the menu, **File > Export To > Ansys SIwave (`*.siw`)**



4.3.3. Cadence Sigrity (*.spd)

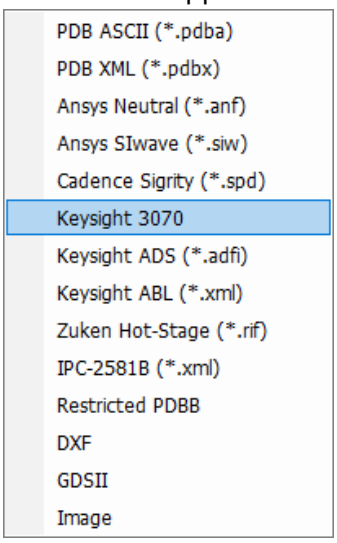
Using this menu, user can export file to be used in Sigrity SPD. To do this work, use the menu, **File > Export To > Cadence Sigrity (`*.spd`).**

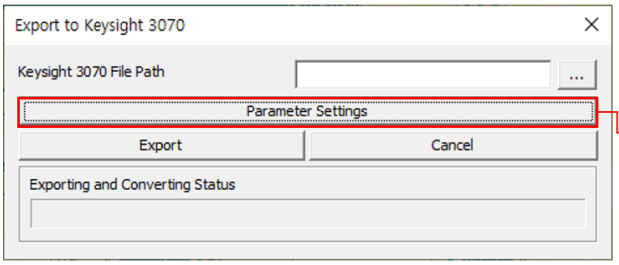


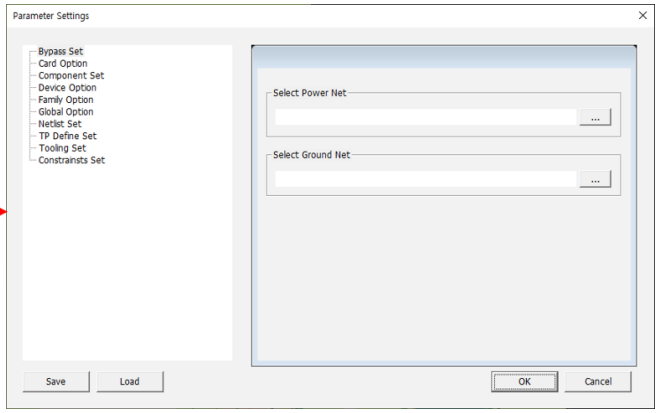
4.3.4. Keysight 3070

Using this menu, user can export file to be used in Keysight 3070. To do this work, use the menu, **PollEx PCB > File > Export To > Keysight 3070.**

PollEx PCB supports AGILENT i3070 format and also exports location report for test point.

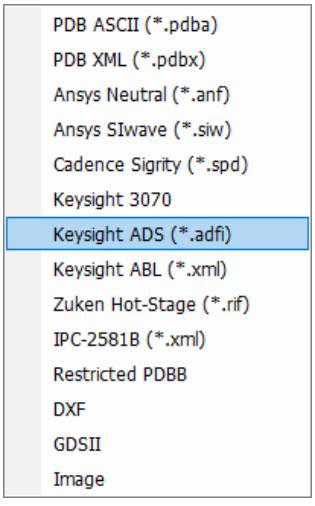


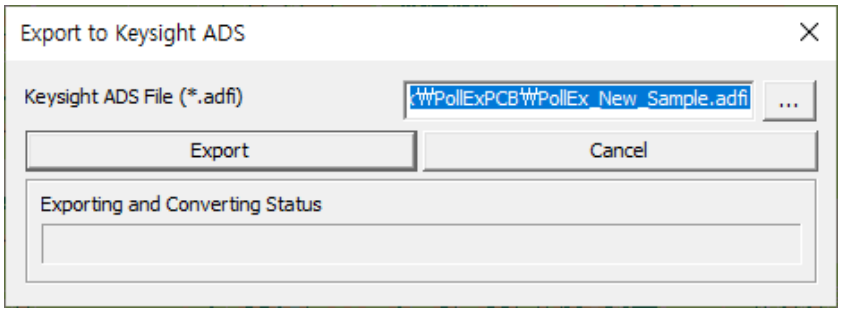




4.3.5. Keysight ADS File

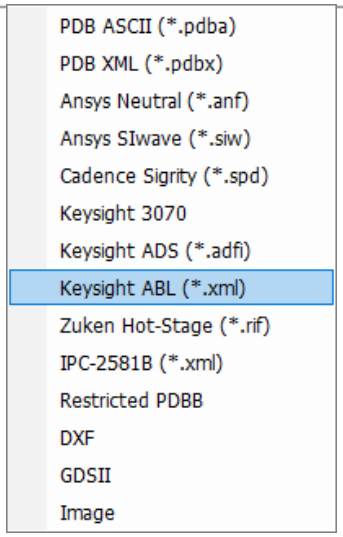
Using this menu, user can export file to be used in Keysight ADS. To do this work, use the menu, **PollEx PCB > File > Export To > Keysight ADS (`*.adfi`).**

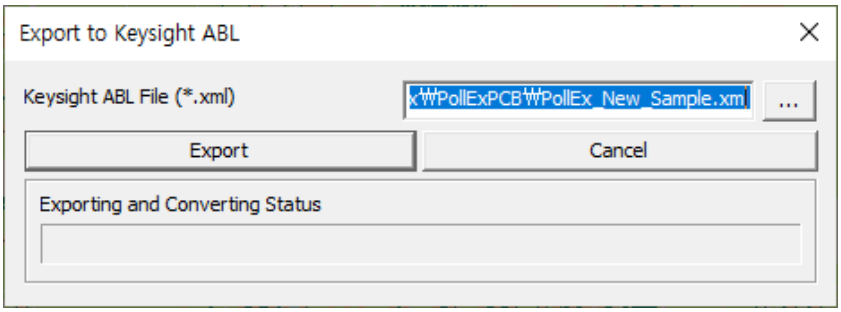




4.3.6. Keysight ABL (*.xml)

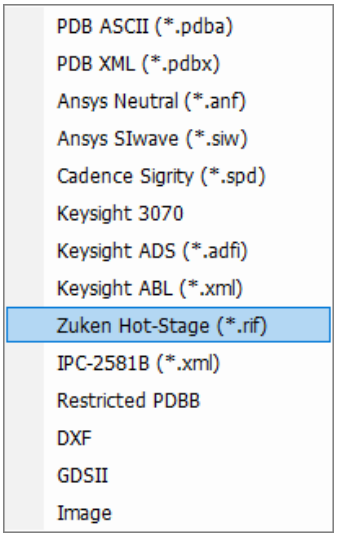
Using this menu, user can export file to be used in Keysight ABL. To do this work, use the menu, **PollEx PCB > File > Export To > Keysight ABL (`*.xml`).**

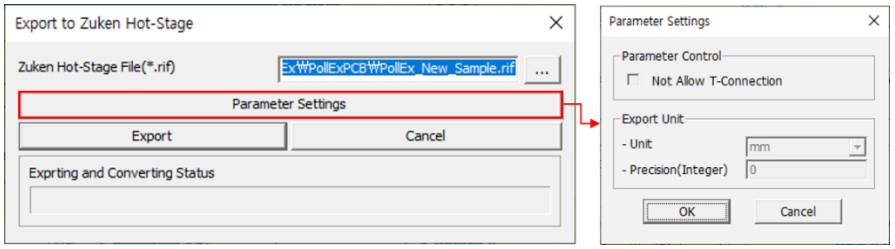




4.3.7. Zuken Hot-Stage (*.rif)

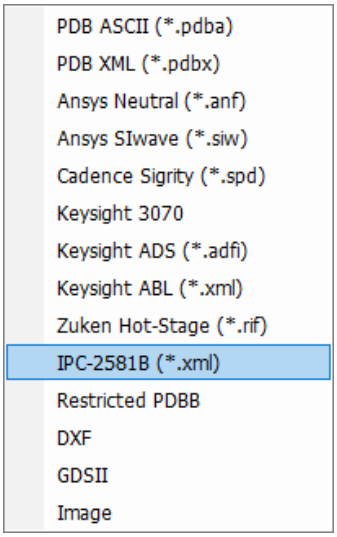
Using this menu, user can export file to be used in Zuken Hotstage. To do this work, use the menu, **PollEx PCB > File > Export To > Zuken Hot-Stage (`*.rif`).**

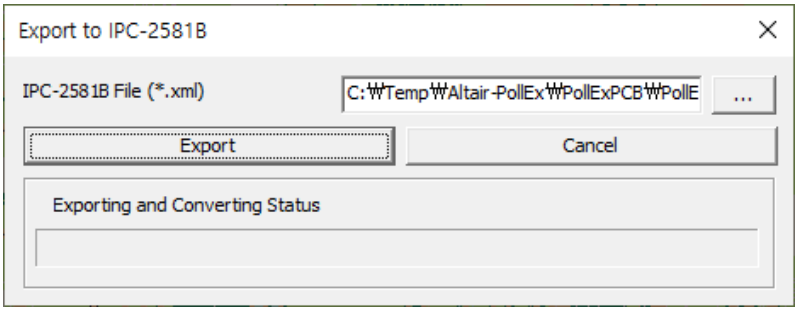




4.3.8. IPC-2581B

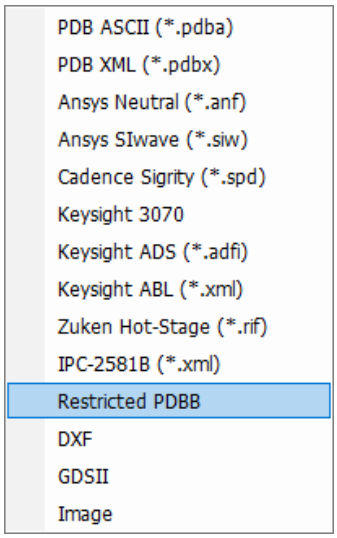
Using this menu, user can export file to be used in IPC-2581. To do this work, use the menu, **PollEx PCB > File > Export To > IPC-2581B.**



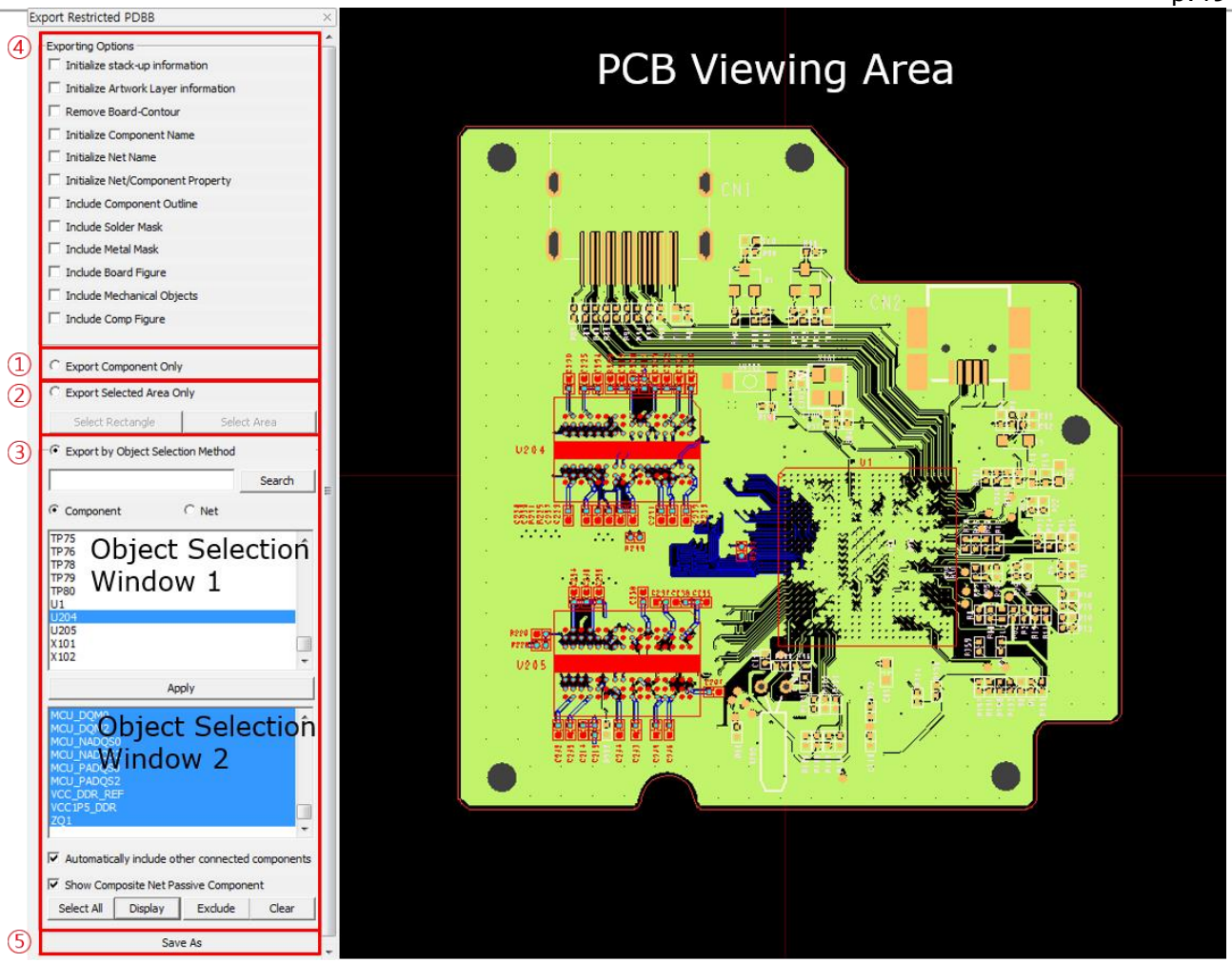


4.4. Restricted PDBB

Using this feature, user can save some parts of whole board, after selecting nets and connected components for selected nets. In case of sending design to outer but if users do not want to whole board with security issues, this feature is effective. Use the menu, **File > Export To > Restricted PDBB**.



Upon launching **Restricted PDBB** menu, user meets following dialog menu to save partial design.



User has three options for saving design. One is saving component placement information only (①). Another is saving selected area only (②) and the other is saving design depending objects and related objects (③).

① Select **Export Component Only** button menu to save design for only components placement. At this status, routing and non-electrical information will be excluded at saving.

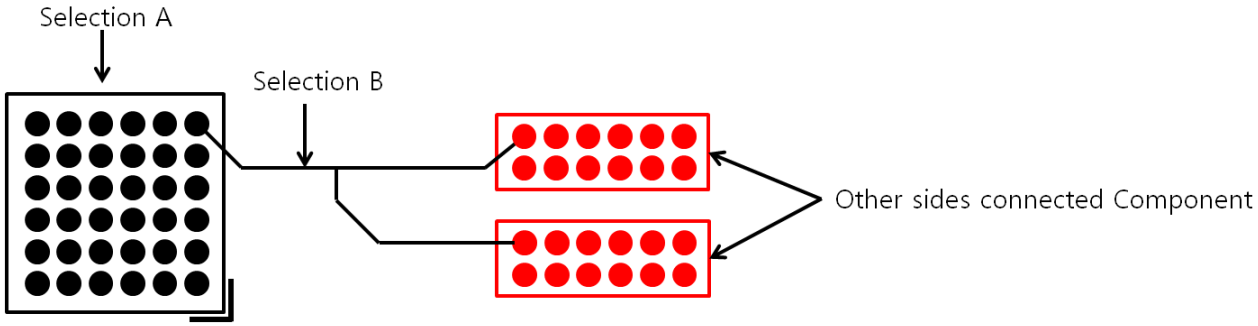
② **Export Selected Area Only** will give users two selection method. One is selecting rectangle area and the other is selecting arbitrary area.

③ **Export by Object Selection Method** will give users two selection menu windows. Combining two windows' selections, user can select objects. If **Window 1** selection is Component, **Window 2** selection will be Net and vice versa. It means user can select component and its connected net and vice versa.

Using **Search** button menu, user can find necessary objects in **Window 1.**

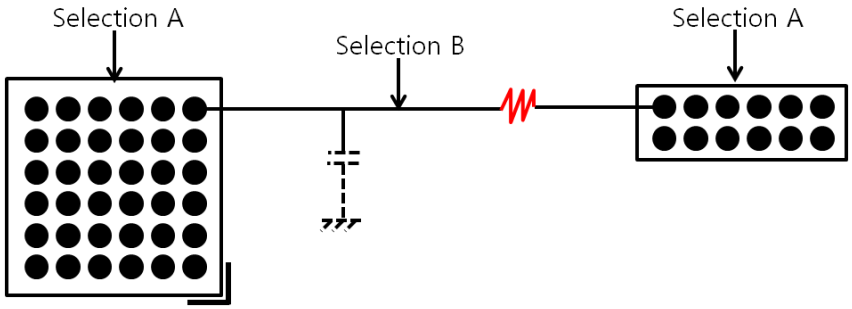
- **Automatically include other connected components**

If **Window 1** selection is Component, **Window 2** selection will be Net automatically. In this case, and if this checking is turn on status, PollEx PCB will save also save include other side component also.



- **Show Composite Net Passive Component**

If user selected components and they are connected with passive device, PollEx PCB will include passive device for saving when this option is turn on status.



- **Select All**

Select all items in **Window 2**.

- **Display**

Show selections on PCB Viewing Area.

- **Exclude**

Show selections on PCB Viewing Area with hidden for unselected objects.

- **Clear**

Reset window display.

④ **Exporting Options**

- **Initialize stack-up information**

Reset stack-up information and make it with default value.

- **Initialize Artwork Layer information**

Reset artwork layer information and make it with default value.

- **Remove Board-Contour**

Remove board contour data and make it with basic rectangle geometries.

- **Initialize Component Name**

Remove all part's name information and rename them with string starting "PartXXX". All other footprint, package and device name will be re-arranged. Vias and padstacks name will be re-arranged also.

- **Initialize Net Name**

Remove all nets' name and rename them with string starting "NetXXX". Vias and padstacks name will be re-arranged also.

- **Initialize Net/Component Property**

Remove all properties assigned to net and components (reference designator).

- **Include Component Outline**

Include all component outline of component (Artwork Layer-201: COC Top, 202: COC Bottom).

- **Include Solder Mask**

Include all solder mask layer.

- **Include Metal Mask**

Include all metal mask layers.

- **Include Board Figure**

Include all board figures.

- **Include Mechanical Objects**

Include all mechanical objects.

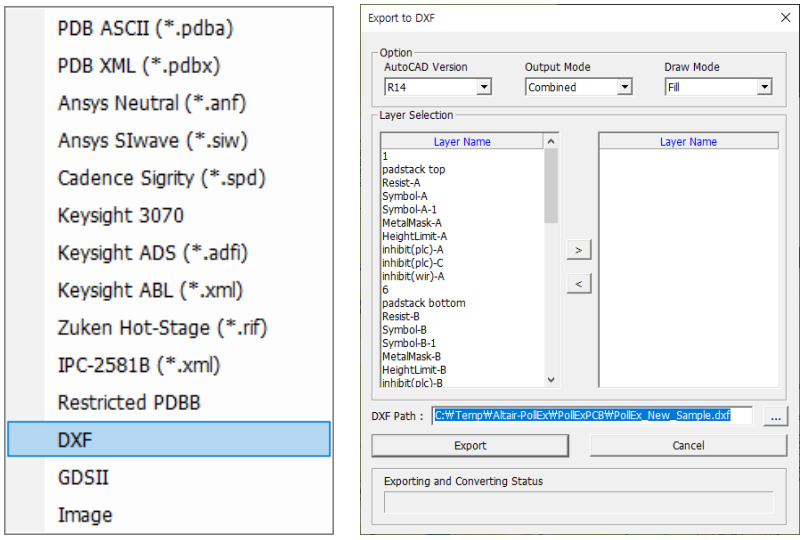
- **Include Comp Figure**

Include all Component Figure Data.

⑤ Using **Save As** menu, save current status into different PDBB file.

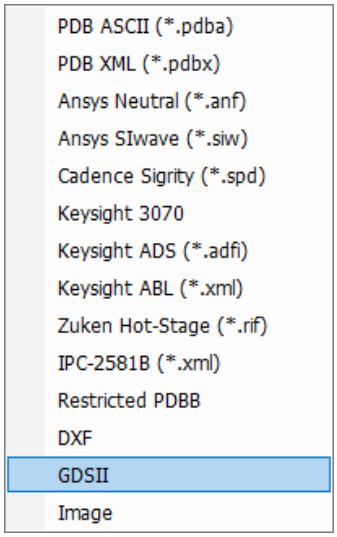
4.5. DXF

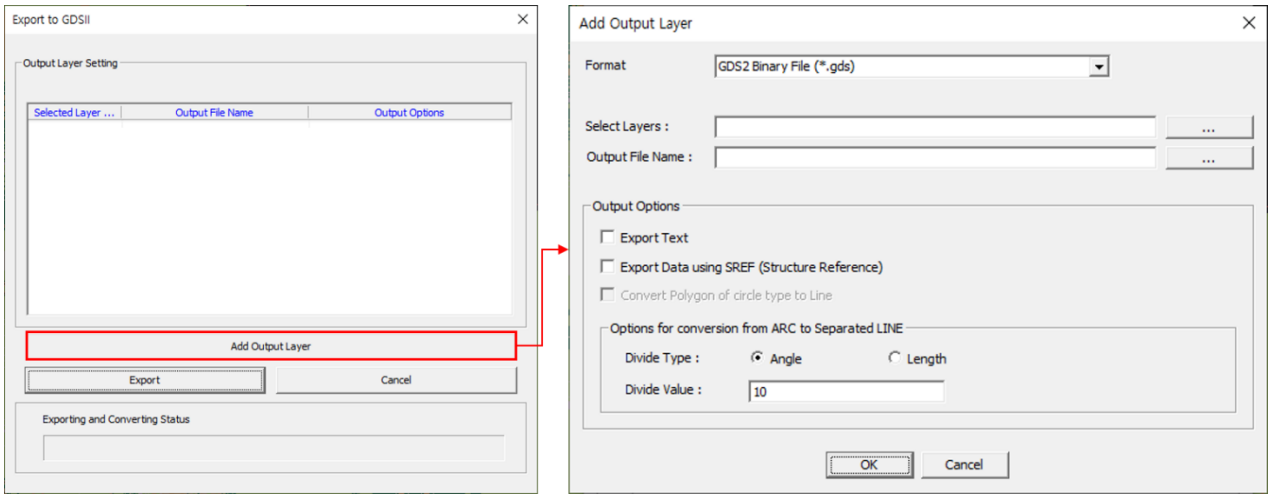
Using this menu, user can export file to be used in DXF. To do this work, use the menu, **PollEx PCB > File > Export To > DXF.**



4.6. GDSII

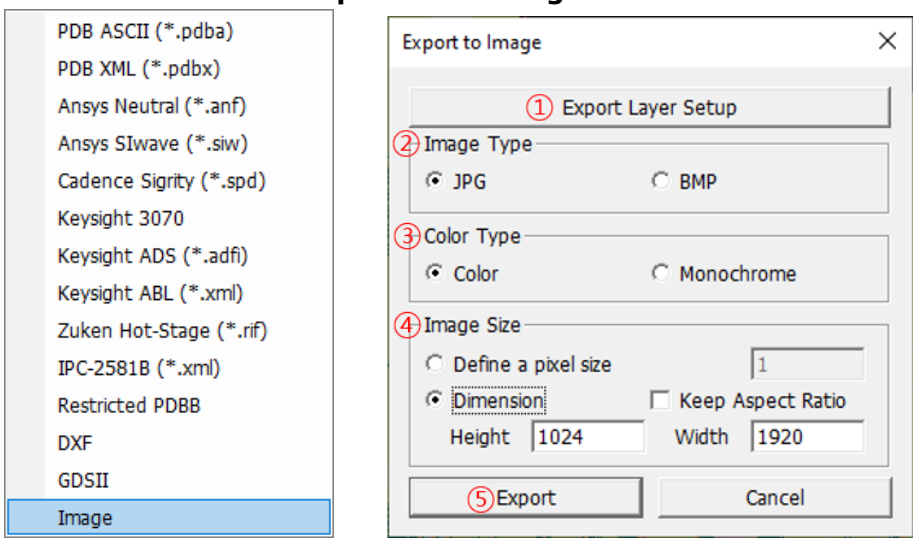
Using this menu, user can export file to be used in GDSII Format. To do this work, use the menu, **PollEx PCB > File > Export To > GDSII.**



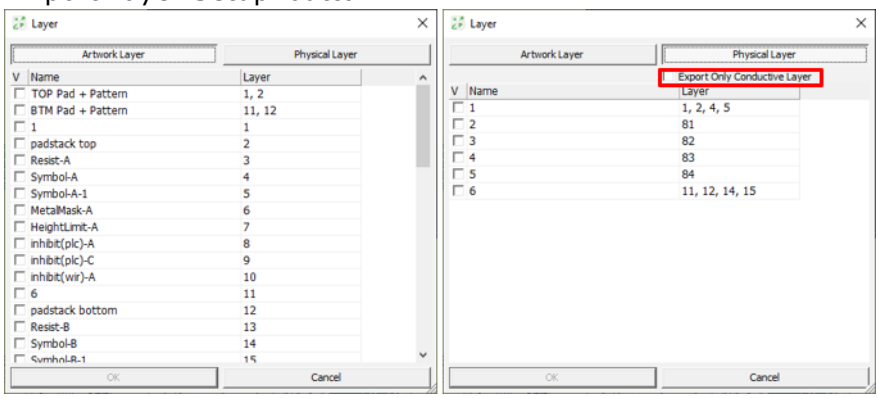


4.7. Image

Using this menu, user can export Image file as * jpg or *.bmp. To do this work, use the menu, **PollEx PCB > File > Export To > Image.**



① **Export Layer Setup:** Select the layer(s) either artwork or physical layers to export by using 'Export Layer Setup' button.



If you select physical layer, 'Export only conductive layer' menu will be enable to include.

② **Image Type:** Select the file type as JPG or BMP.

③ **Color Type:** Select a color type as Color or Monochrome.

④ **Image Size:** Set the image size.
Define a pixel size: Set an each pixel size.
Ex.) If you have a board size as 100x100, and then set the value as 0.1. It will be exported as 1000x1000. (The current unit in PCB design will be used.)
Dimension: Set the image size according to given resolution value as Height and Width.
Keep Aspect Ratio: By using this option, the image size will be calculated automatically with considering actual board size and given dimension value.

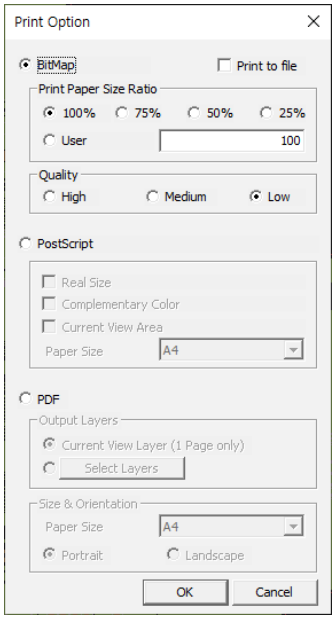
⑤ **Export:** You can get the exported image with clicking this button.

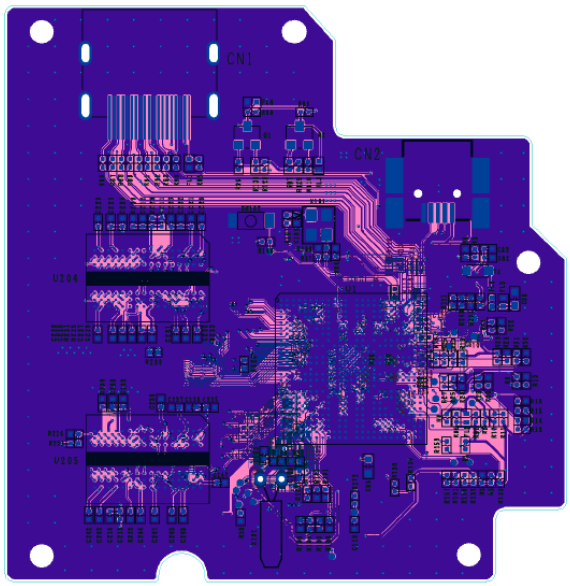
5. Print

PollEx PCB's print feature supports three types of formats.

5.1. Bitmap

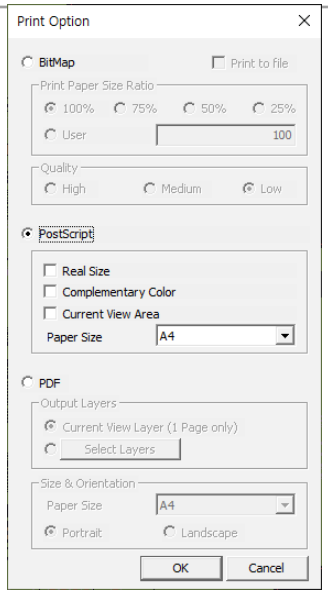
Use the menu, **File > Print**.
Print Paper Size Ratio Size ratio regarding to the PCB.
Quality: The scale of resolution.





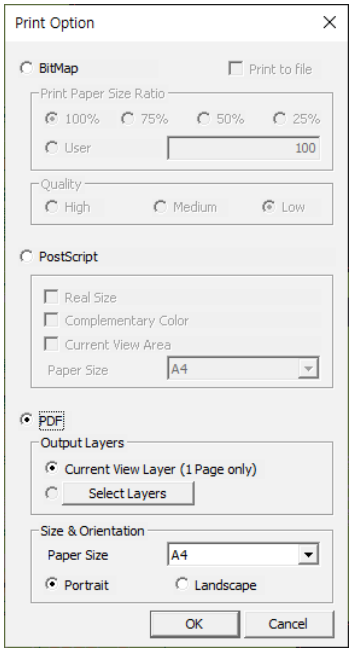
5.2. PostScript

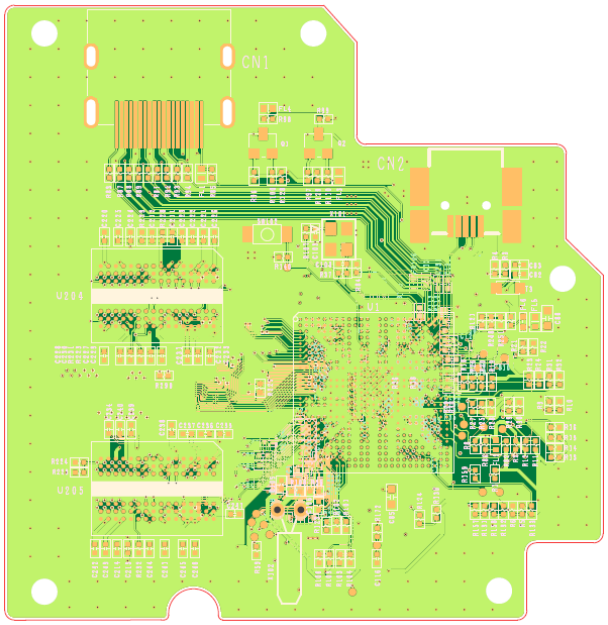
To print out postscript file, use the menu, **File > Print**.
Real Size: Print out size as same as the real PCB size.
Complementary Color: Define the color of printing.
Current View Area: Print out same as viewing status.



5.3. PDF

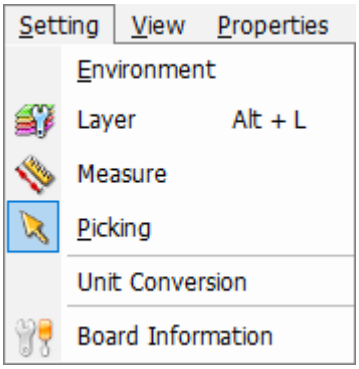
To print out with PDF format, use the menu, **File > Print**.
Paper Size: Select the paper size.





Setting

Under the setting menu, there are many setting items for defining default value for using PollEx PCB. Use the menus under **Setting** in main menu.

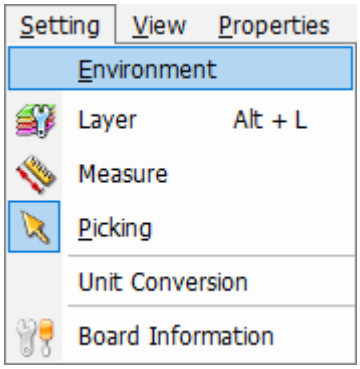


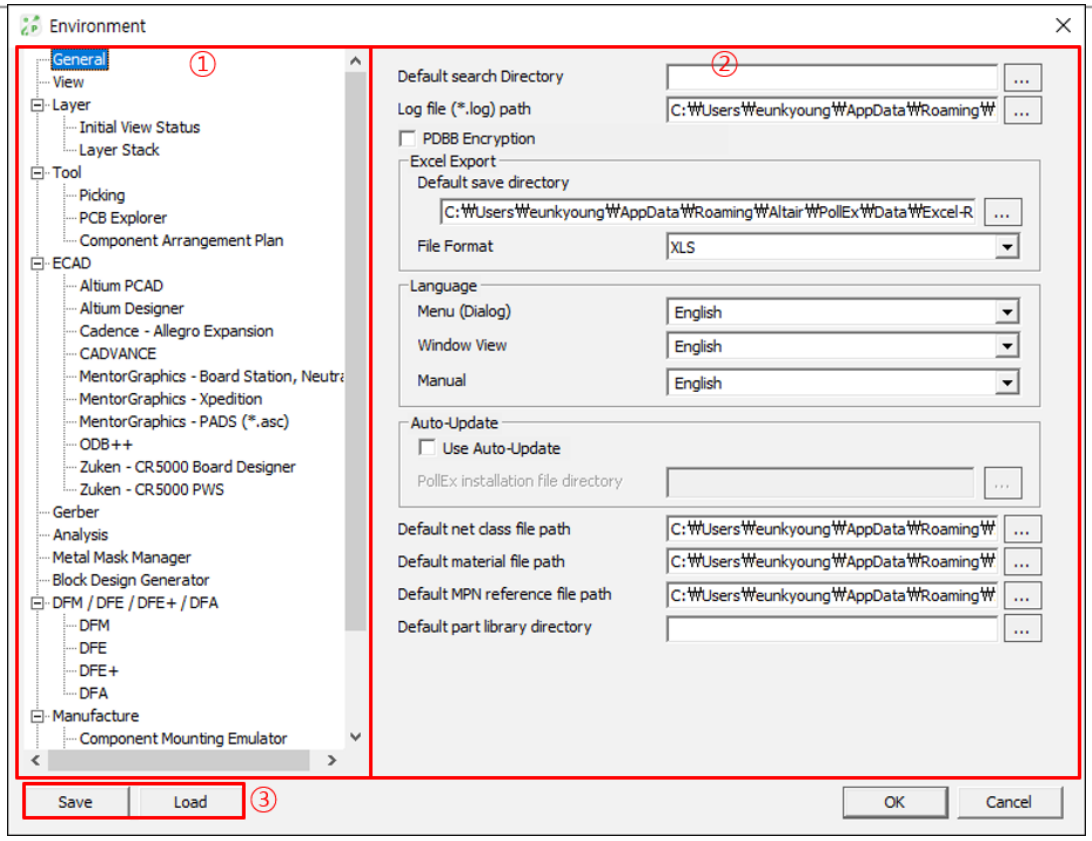
1. Environment

Using this menu, users can set-up defaults for using PollEx PCB. Setting items are as follows;

- Whether user set password during saving operation for design open
- Working file path
- Display method
- Default language for menu and manual
- Default setting for different ECAD reader

Use the menu, **Setting > Environment**.

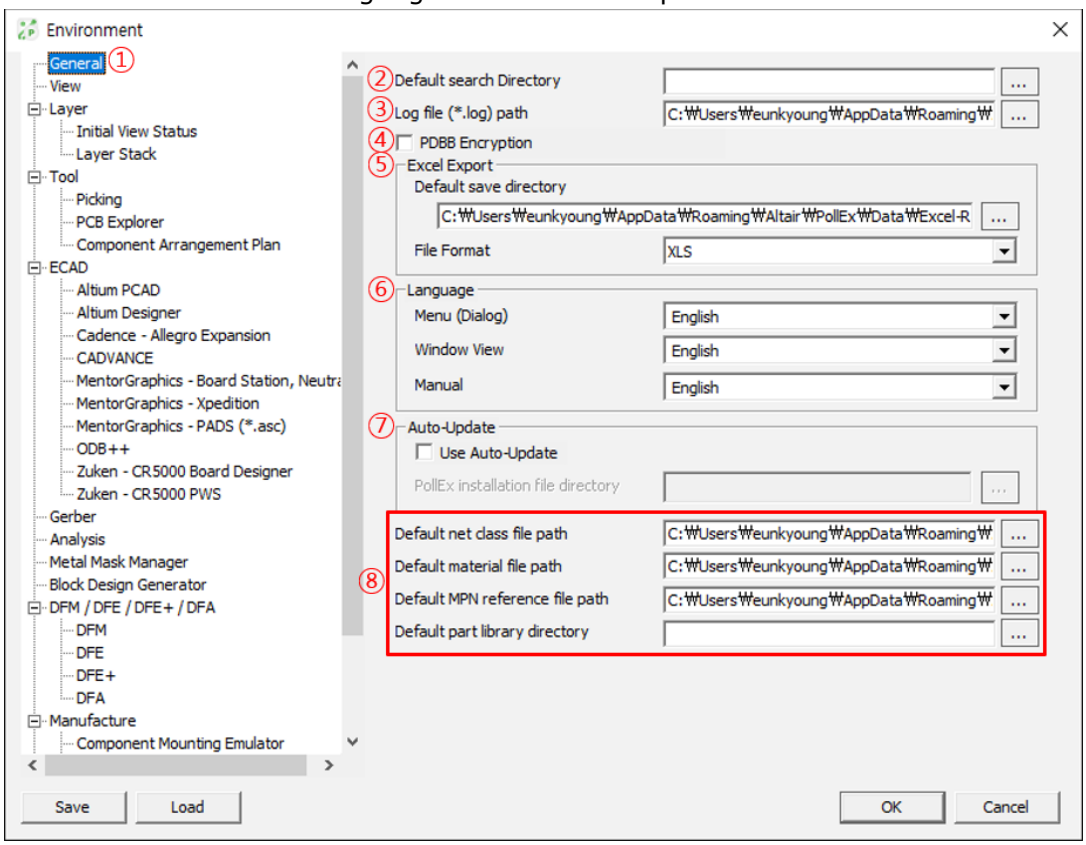




① Classification for environment setting items.
② Each item's parameter setting window.
③ User can load or save environment setting. So multiple users can share setting to use same environment.

1.1. General

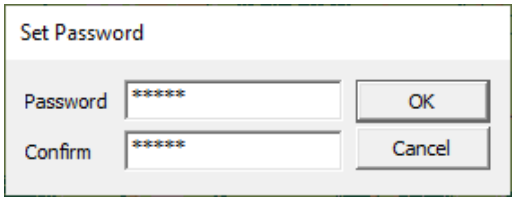
① **General**: User can set language and default file path.



② **Default search Directory**: Set default file open path for PollEx PCB.

③ **Log File (*.log) path**: Set default log file saving path.

④ **PDBB Encryption**: Define whether to use encryption when saving PDBB file. If user checks this option, user may meet following password input window before saving file.



⑤ **Excel Export**: Set default MS/Excel export path and default export format such as csv, xls or xlsx.

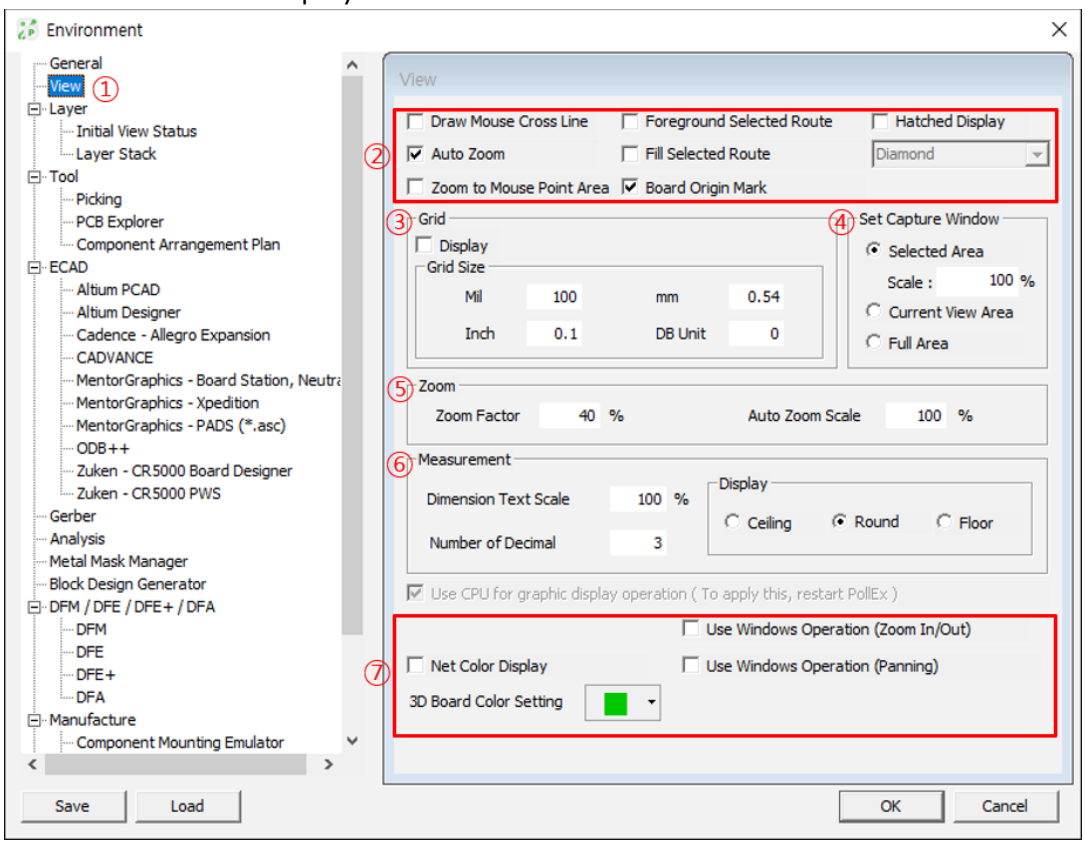
⑥ **Language**: Default language for Menu, Window View and Manual is English.

⑦ **Auto Update**: Set default directory of Install file location.

⑧ **- Default net class file path**: Set default net class file path.
- **Default material file path:** Set default material file path.
- **Default MPN reference file path:** Set default MPN reference file path.
- **Default part library directory:** Set default part library directory.

1.2. View

① **View**: Set window display.



② **Draw Mouse Cross Line**: Mouse pointer shows with "+" mark.
Foreground Selected Route: During picking operation, selected pattern will be shown at the top if there are multiple patterns are overlapped.
Hatched Display: Display polygons to hatch as Forward Diagonal / Backward Diagonal / Cross / Diamond / Vertical /Horizontal.
Auto Zoom: Upon using PCB Explorer, Highlight or Exclude operation shows objects with auto zoom-in.
Fill Selected Route: Show selected routing pattern with filled shape.
Zoom to Mouse Point Area: Zoom area based on mouse point.
Board Origin Mark: Display the board origin mark

③ **Grid**: Set the distance of grid and decide whether PollEx PCB shows grid or not.

④ **Set Capture Window**: Use the menu to make partial image capture, screen capture, full area capture.

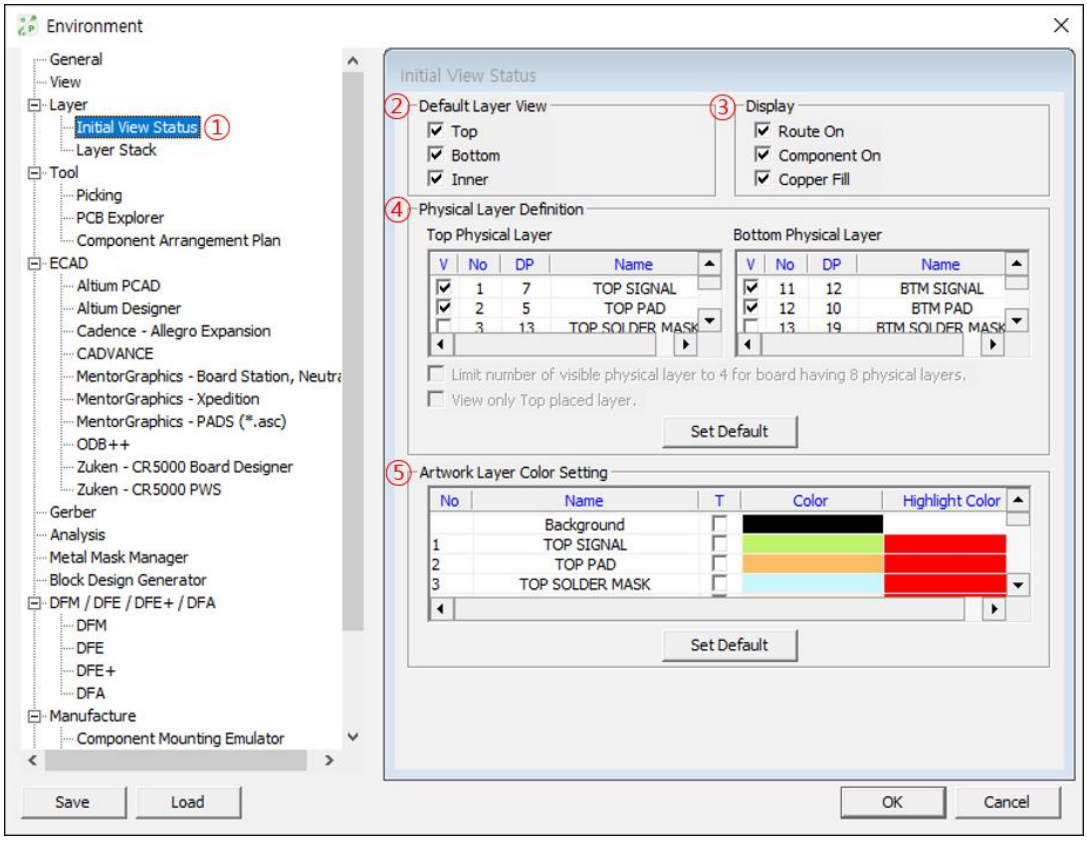
⑤ **Zoom**: Specify the zoom ratio.

⑥ **Measurement**
Dimension Text Scale: Set the dimension's size using measure function.
Decimal Point: Set the decimal point for measure resulting. Select the value 1~5.
Display: Select one among ceiling, round and floor for the decimal point.

⑦ **Net Color Display**: If source ECAD file has its original color settings for routing nets, this option will decide whether PollEx PCB show original ECAD color or use default PollEx PCB color.
User Windows Operation: For zoom In/Out and panning operation, operations will be applied reversely.

1.3. Layer - Initial View

① **Initial View**: Set the default PDBB file's open status for color, display and layer display on/off status.



② **Default Layer View**: Set layer's displaying status for top/bottom/inner layers. For the huge file size, checking top only is very effective for opening speed.

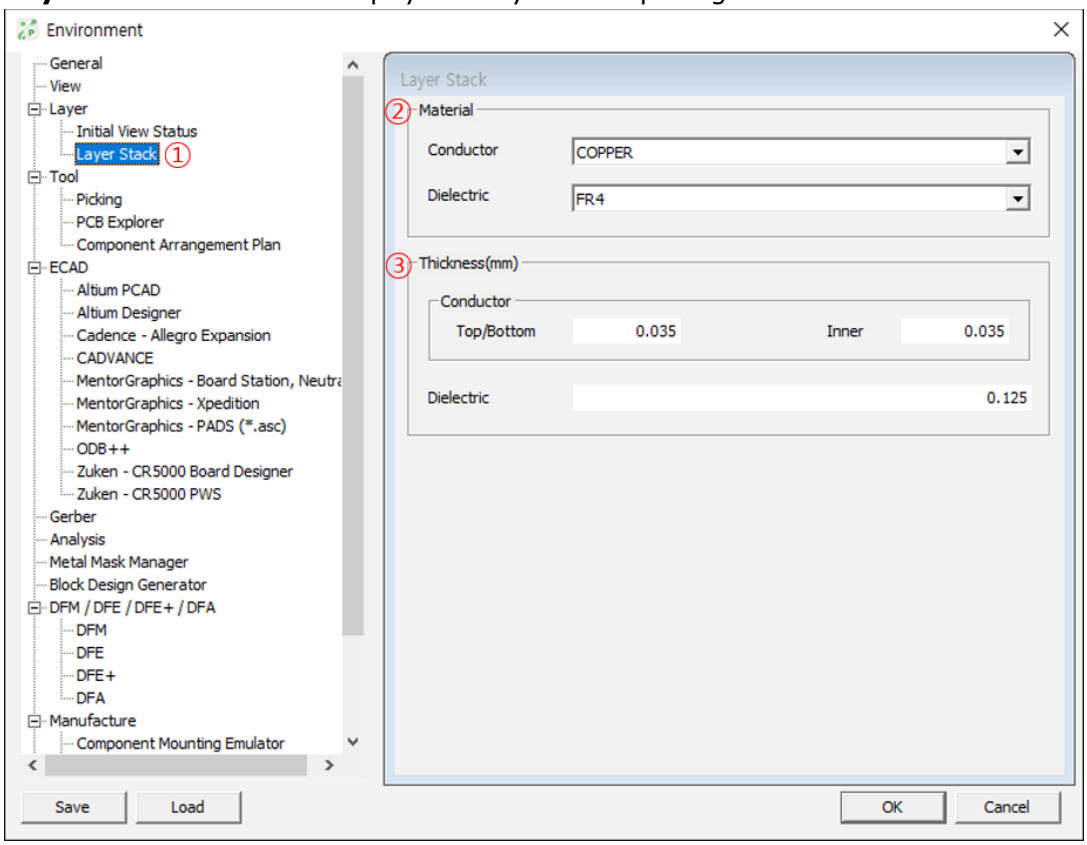
③ **Display**: For objects on PCB, set the objects showing status.
Route On: Initially PollEx PCB display routing pattern.
Component On: Initially PollEx PCB display components.
Copper Fill: Initially PollEx PCB shows copper pour as filled shape.

④ **Physical Layer Definition**: Decide for showing top/bottom component related layer displaying status.

⑤ **Artwork Layer Color Setting**: PollEx PCB can define the artwork layers' default color. User can highlight some specific layers to change color.

1.4. Layer-Layer Stack

① **Layer Stack**: Set the PCB physical layer's composing materials.

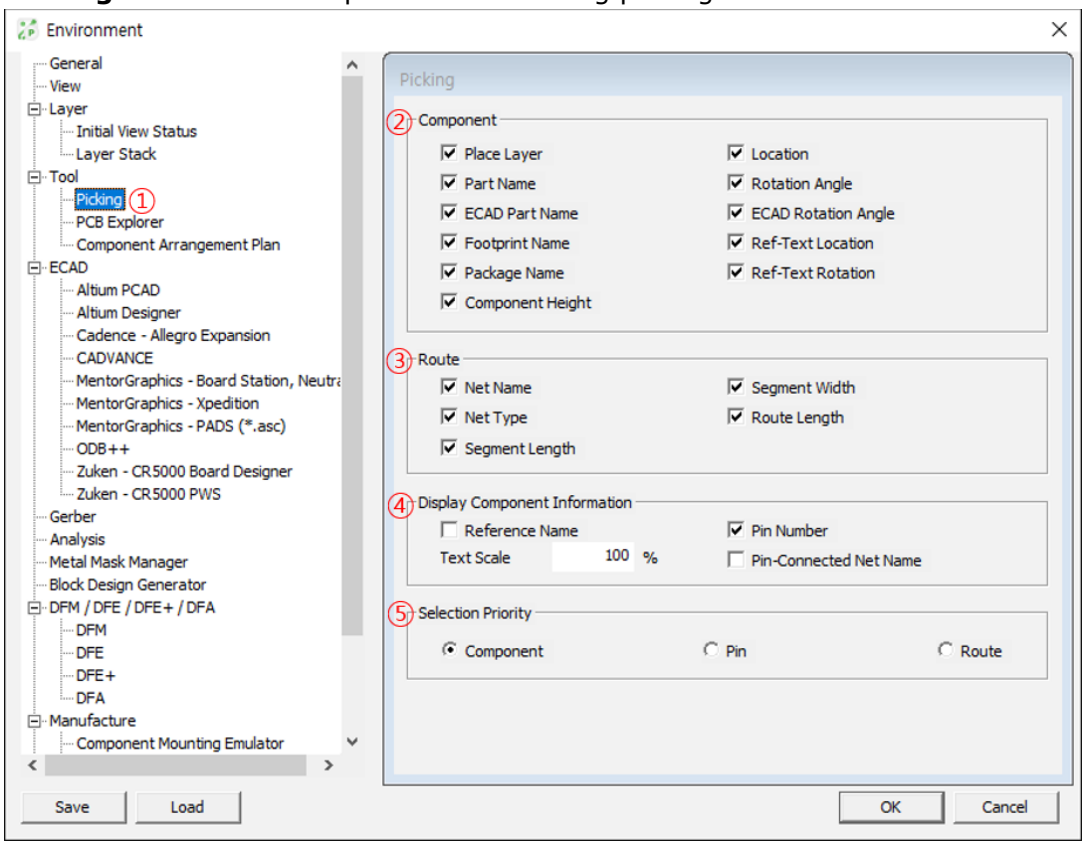


② **Material**: Define the PCB's conducting and di-electric material from material library.

③ **Thickness**: Define the conducting layer's default thickness values.

1.5. Tool - Picking

① **Picking**: Set the default parameter for using picking tool.



② **Component**: Display what attributes are displayed when picked a component.

③ **Route**: Display what attributes are displayed when picked a route.

④ **Display Component Information**

Reference Name: Specify whether to show reference name in picking tool operation.

Pin Number: Specify whether to show pin number in picking tool operation.

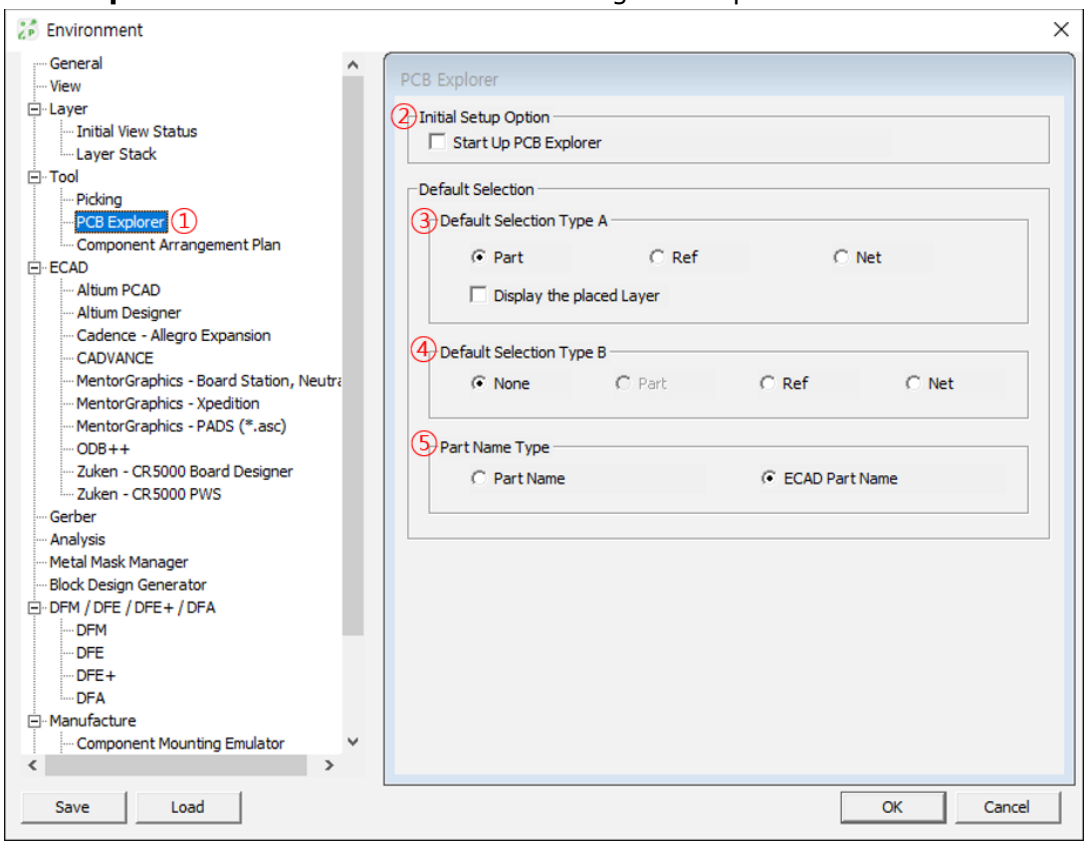
Pin-Connected Net Name: Specify whether to show pin-connected net name in picking tool operation.

Text Scale: Set text scale.

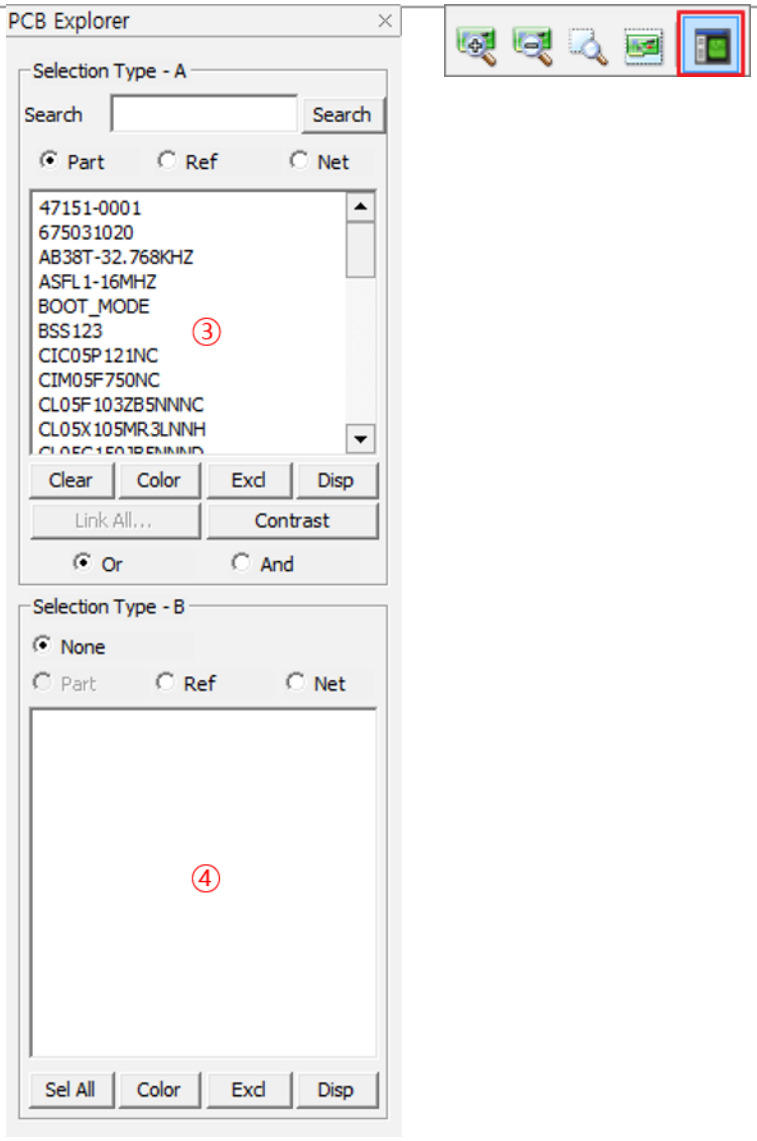
⑤ **Select Priority**: Select priority among component, pin and route.

1.6. Tool - PCB Explorer

① **PCB Explorer**: Set the default value for using PCB Explorer.



② **Initial Setup Option**: If this option is checked, PCB Explorer will be launched after opening PollEx PCB job file.

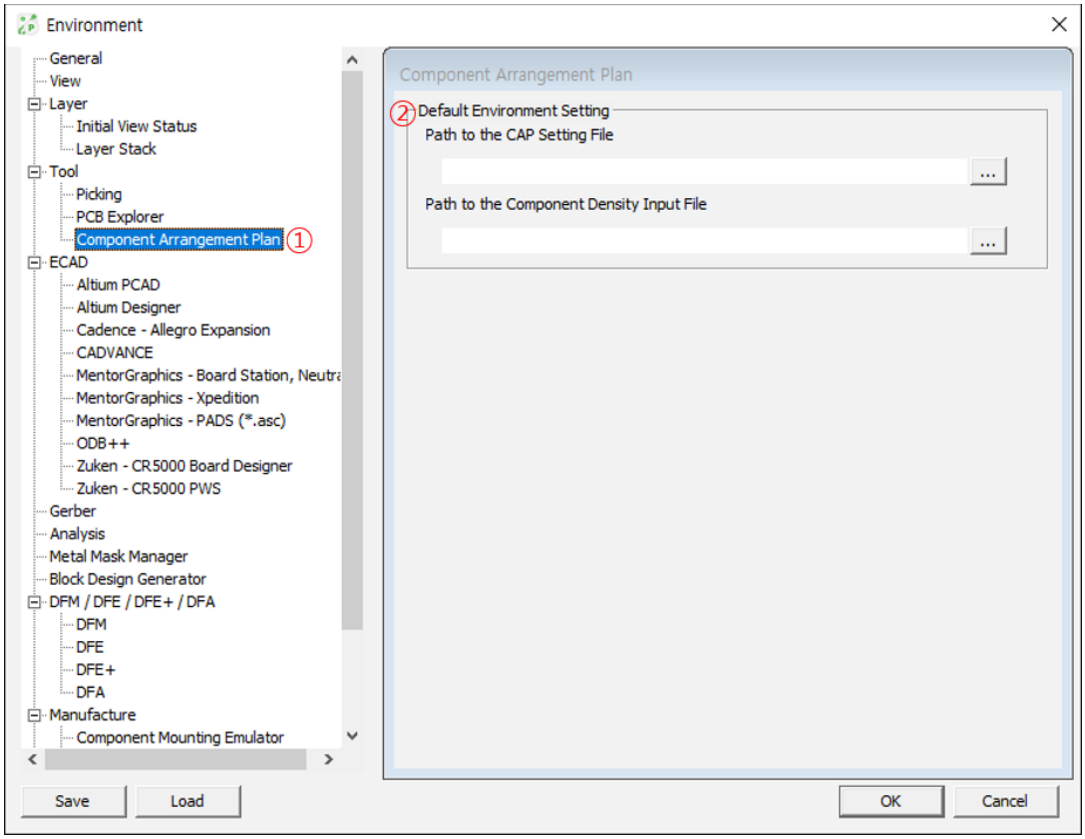


③ Set the default selection Type A when launched the PollEx Explorer.
④ Set the default selection Type B when launched the PollEx Explorer.
⑤ In PDB data structure, there are two name properties, part name and ECAD part name. If there is broken component case, unique identifier, part name will be given differently than that is assigned in ECAD tools. Decide what name will be used in part selection window.

1.7. Tool – Component Arrangement Plan

① **Component Arrangement Plan**: Set the default values for using the Component Arrangement Plan tool.

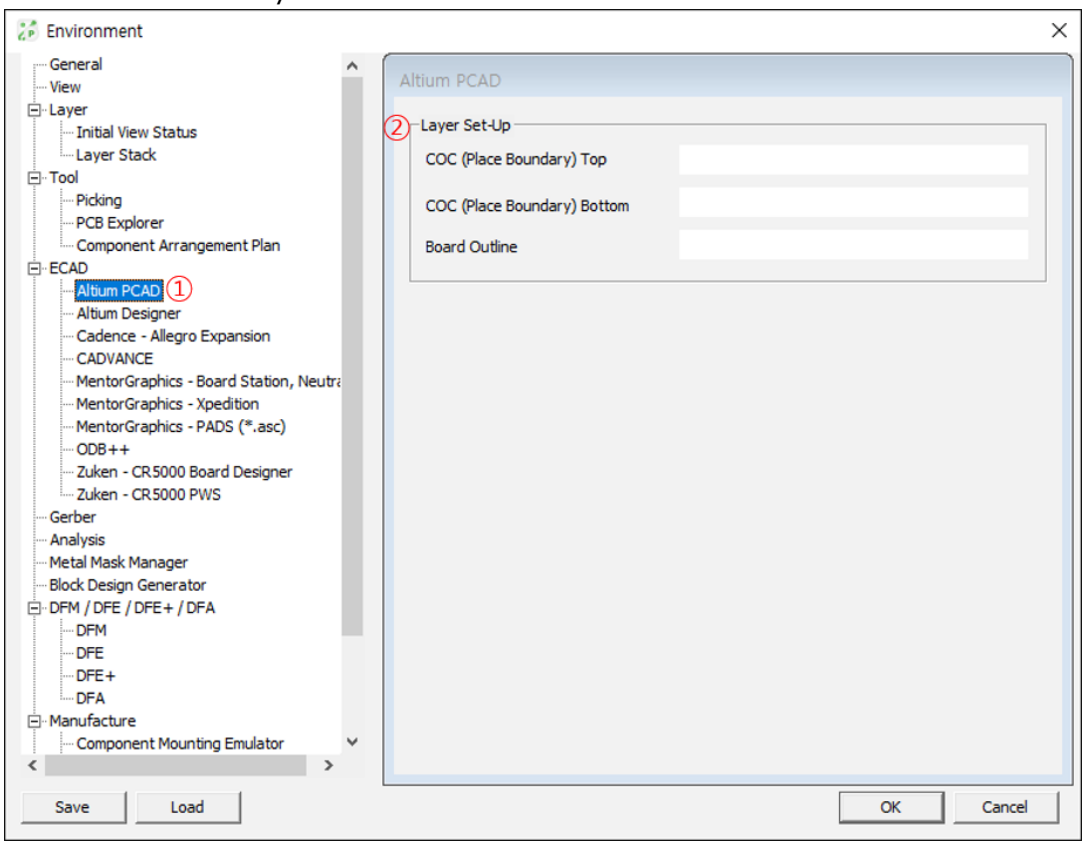
② **Default Environment Setting**: Set environment file, `*.cpas` and input file path.



1.8. ECAD - Altium PCAD

① **Altium PCAD**: Default environment setting to import Altium PCAD.

② **Layer Set-up**: Set Altium layers' name which will be used as PDB's component outline layer and board outline layer.

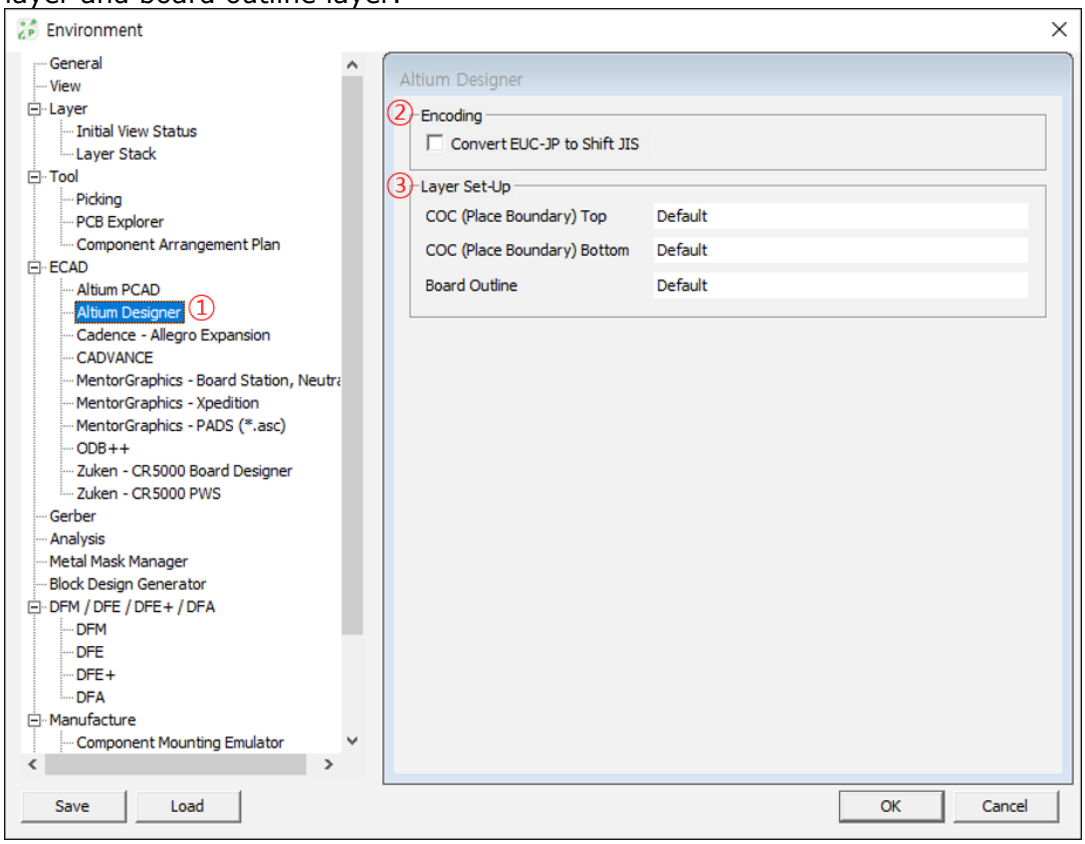


1.9. ECAD - Altium Designer

① **Altium Designer**: Default environment setting to import Altium Designer.

② **Encoding**: Check this option if converting EUC-JP to Shift JIS.

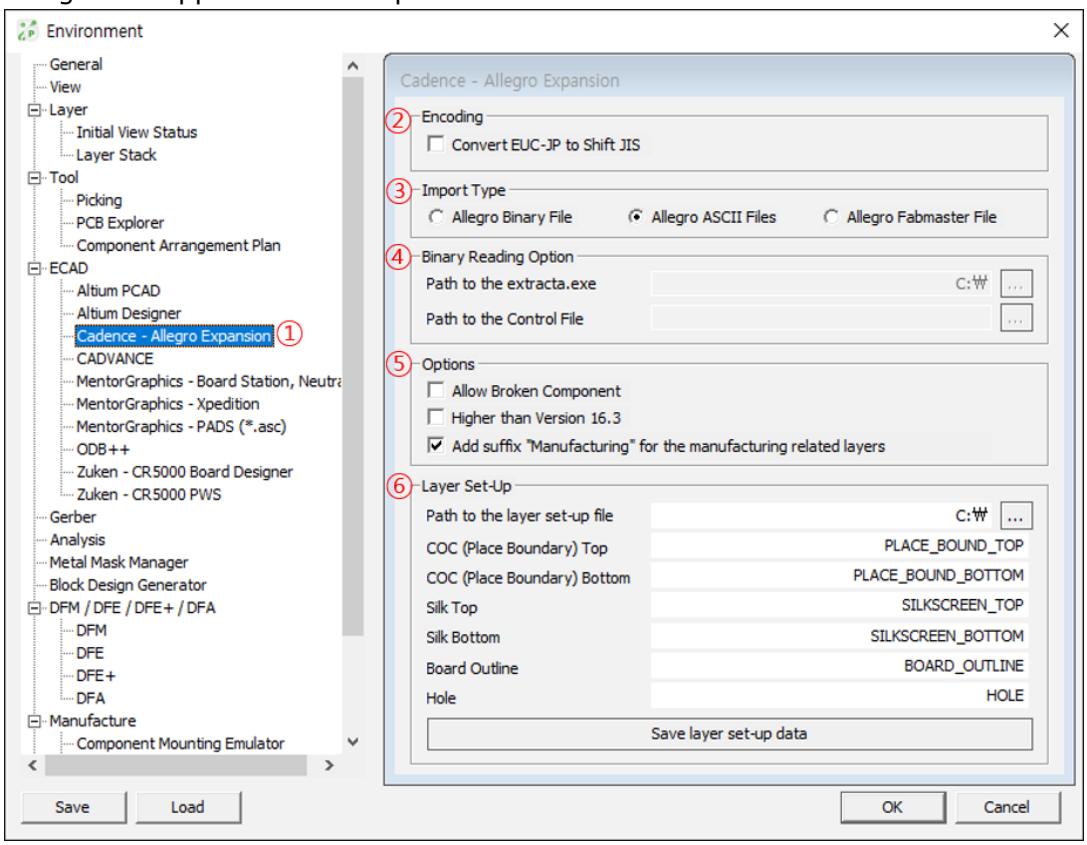
③ **Layer Set-Up**: Set Altium layers' name which will be used as PDB's component outline layer and board outline layer.



1.10. ECAD - Cadence Allegro Expansion

Cadence Allegro doesn't support ASCII out feature, but support command utility, `extracta.exe`. The `extracta.exe` is impossible to run alone. It require Allegro installation environment. But it does not ask any license.

① **Cadence Allegro Expansion**: Default environment setting to import Cadence Allegro design for support abnormal pads.



② **Encoding:** while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

③ **Import Type**
Read from Binary File: Support default as Allegro binary file reading.
Read from ASCII File: Support default as Allegro ASCII file reading.
Read form Fabmaster File: Support default as Allegro Fabmaster file reading.

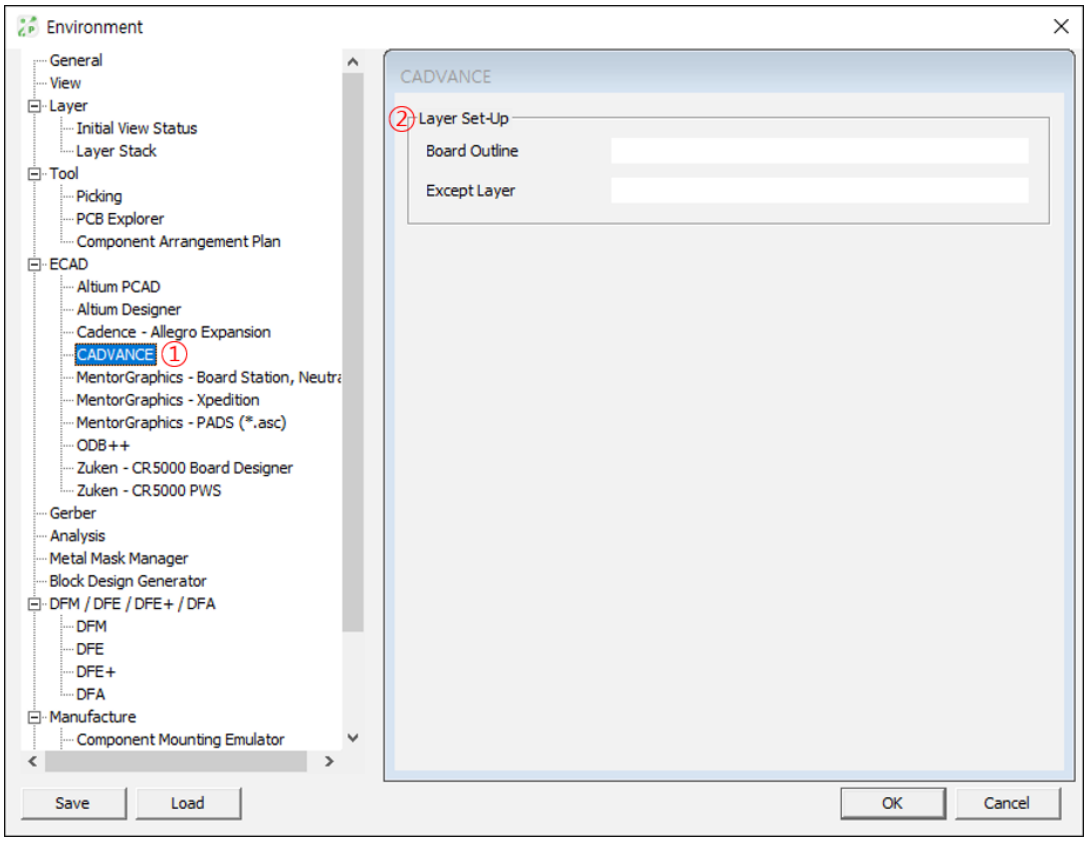
④ **Binary Reading Option**
Path to the extra.exe: Set the file path for Allegro ASCII extraction command utility, `extracta.exe`. In general case, this file location is `%ALLEGRO_INSTALL_PATH%\tools\pcb\bin`.
Path to the Control File: set the path for Allegro ASCII extraction command control file, `AllegroExpansion_ExtractCommandFile163.txt`. In general case, this file is in `C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share\AllegroExpansion_ExtractCommandFile163.txt`.

⑤ **Allow Break Component**: Check when user wants to import Break Component.
Higher than Version 16.3: check this option while reading upper Allegro version than 16.3.

⑥ **Layer Set-Up**: Set Allegro layers' name which will be used as PDB's component related layers for silkscreen, component outline layer.

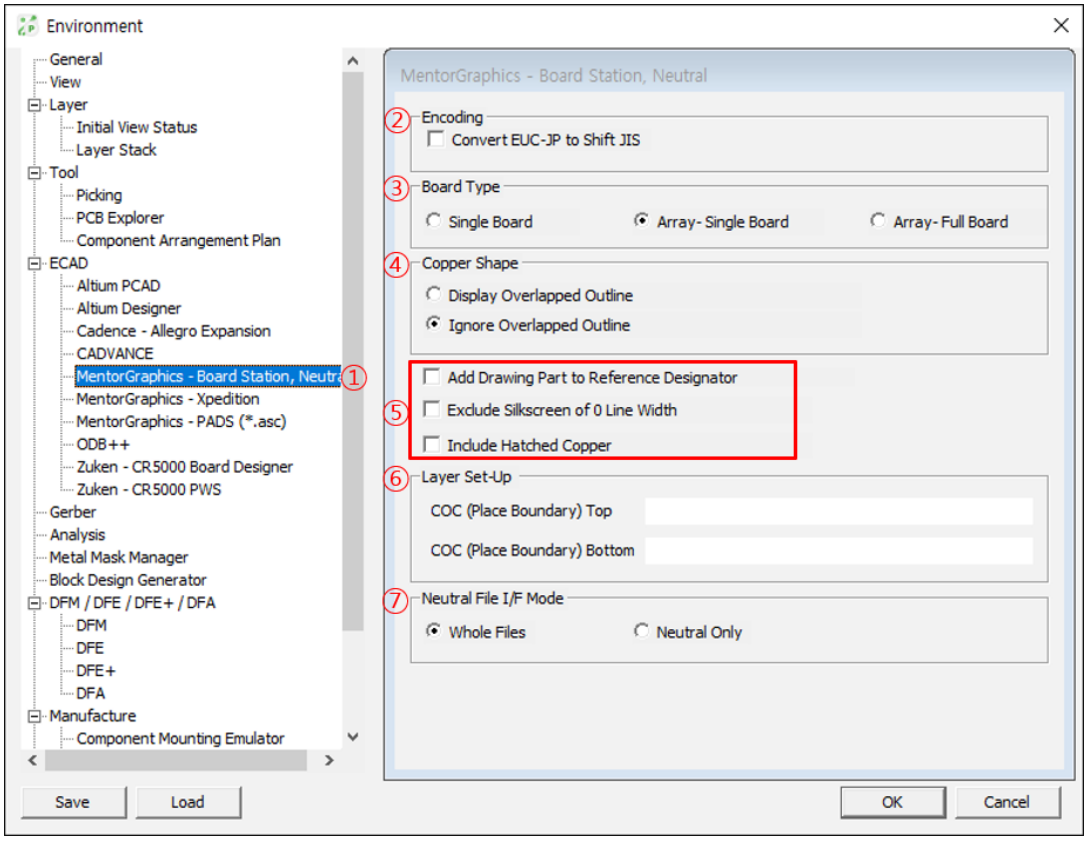
1.11. ECAD - CADVANCE

① **CADVANCE**: Set default value for reading design from CADVANCE file.
② **Layer Set-Up**: Set CADVANCE layers' name which will be used as PDB's component related layers for board outline layer.



1.12. ECAD - Mentor Board Station, Neutral

① **MentorGraphics Board Station, Neutral**: Set default value for reading design from Mentor Graphics Board-Station file.



② **Encoding:** while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

③ **Board Type**
Single: Single board reading.
Array-Single Board: Arrayed board reading but for same type board, read one.
Array-Full Board: Arrayed board reading.

④ **Copper Shape**: For Board-Station design's copper line, decide whether display overlapped dummy line or not.

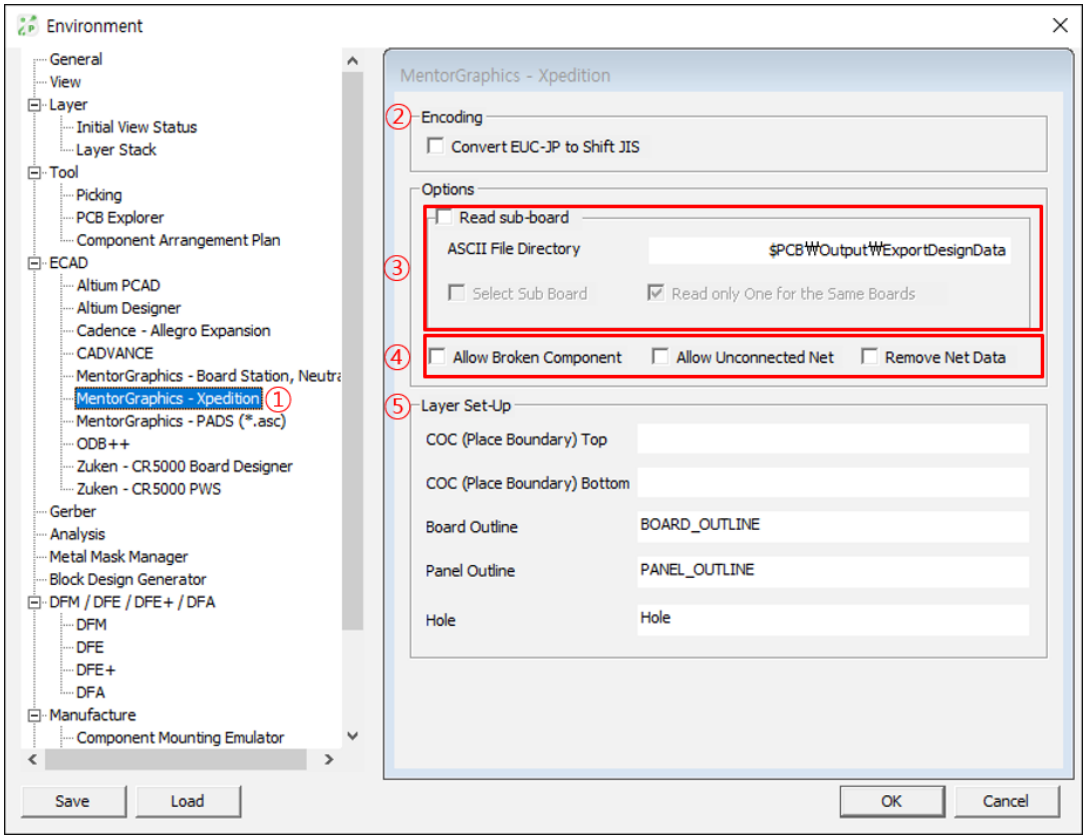
⑤ **Add Drawing Part to Reference Designator**: Add drawing data as part.
Exclude Silkscreen of 0 Line Width: Excludes silkscreen having a line width of zero.
Include Hatched Copper: Check this option if the hatched copper is used in the design.

⑥ **Layer Set-Up**: Set Mentor Graphics Board-Station and Neutral files layers' name which will be used as PDB's component related layers for component outline layer.

⑦ **Neutral File I/F Mode**: Set the interface mode for Neutral files.
Whole Files: Read all of files.
Neutral Only: Read the component section only.

1.13. ECAD - MentorGraphics Xpedition

① **MentorGraphics Xpedition**: Set the default reading parameter for Mentor Graphics Xpedition design.



② **Encoding**: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

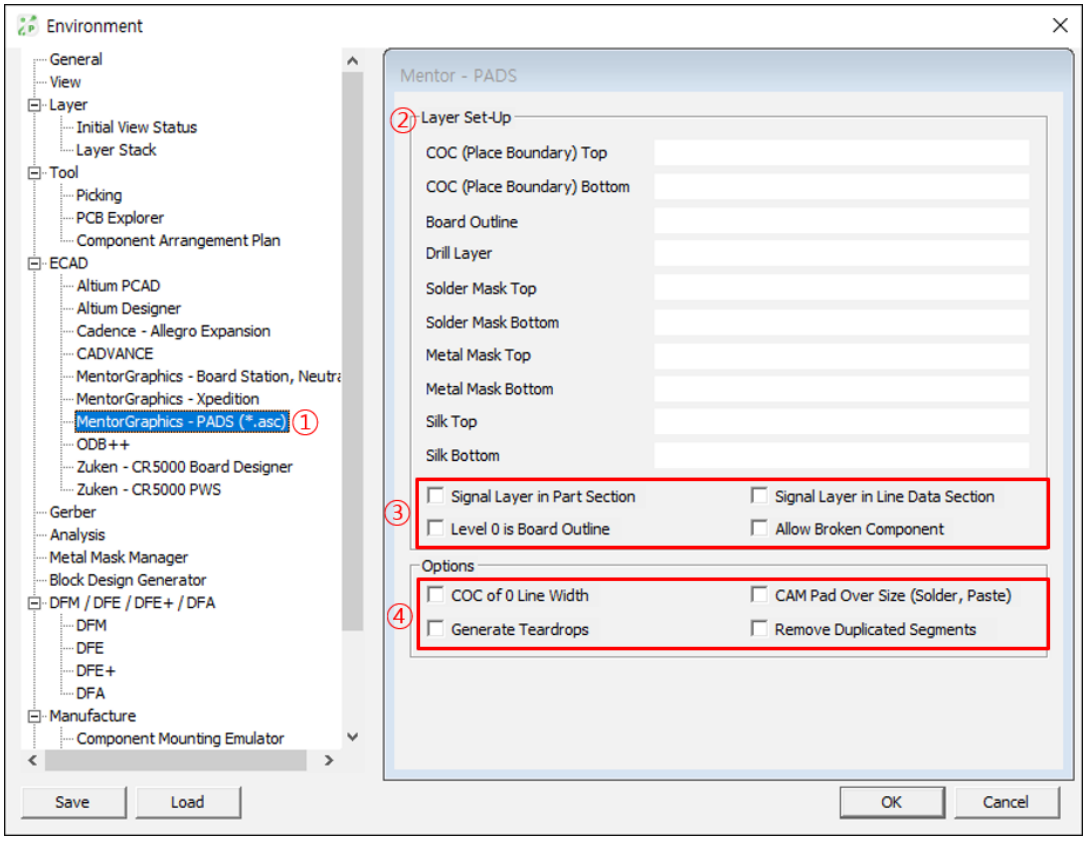
③ **Read sub-board**: Check this option when board is arrayed board.
User Defined ASCII Directory: If there is sub-board in array board, define the location of sub board file data.
Select Sub Board: Option to read the Sub Board.
Read only One for the Same Boards: Only read one board if there are same multiple boards.

④ **Allow Broken Component**: Check this option when user wants to convert reference-changed component to break component.
Allow Unconnected Net: Check this option when user wants to read unconnected net together.
Remove Net Data: Use this option when user wants to import design without routing information.

⑤ **Layer Set-Up:** Set Mentor Graphics layers' name which will be used as PDB's component related layers for component outline layer, board outline layer.

1.14. ECAD - PADS

① **MentorGraphics PADS**: Set the default reading parameters for Mentor Graphics PADS design.



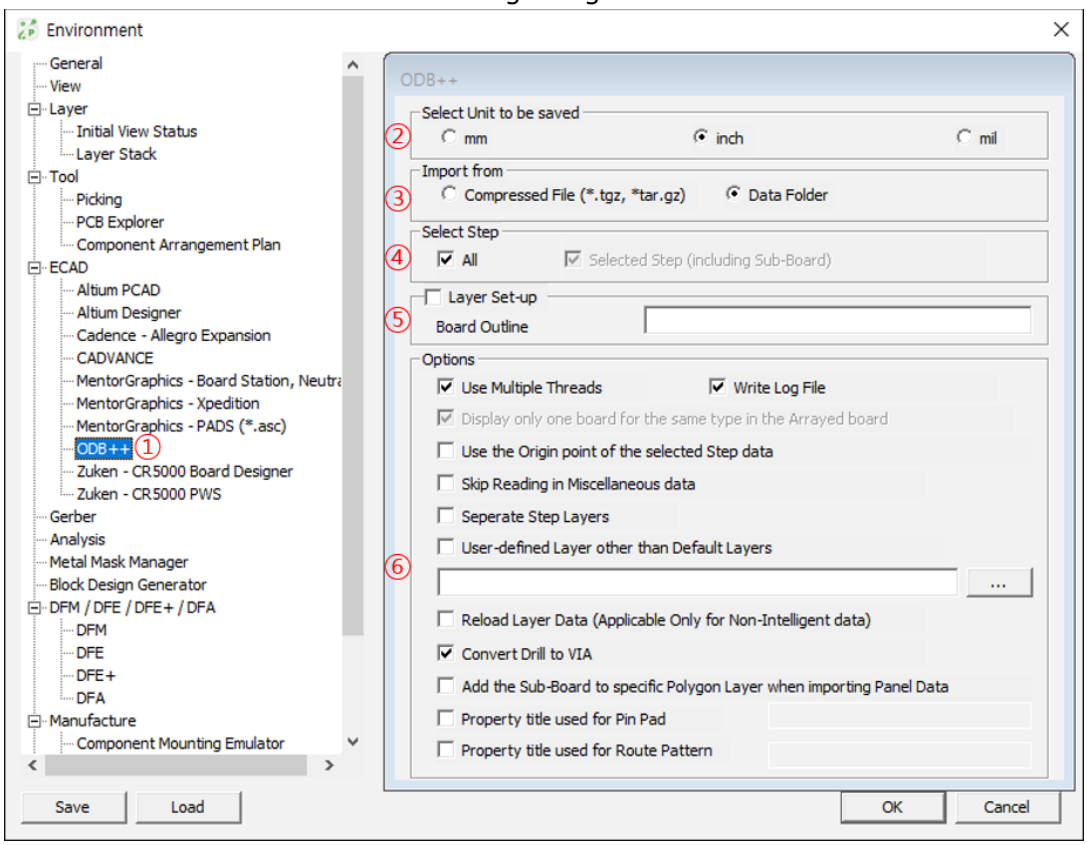
② **Layer Set-up**: Set specific purpose layer names which are used in PADS design. To use in DFM for component's measuring base, it is recommended to set all parameters here.

③ **Signal Layer in Part Section**: In footprint definition, check this option if object layer is signal layer.
Signal Layer in Line Data Section: In board figure definition, check this option if object layer is signal.
Level 0 is Board Outline: Check this option if layer level 0 is board contour layer.
Allow Broken Component: Check this option if Broken Component is used.

④ **COC of 0 Line Width**: Check this option if line width of COC as 0.
CAM Pad Over Size: Check this option if solder mask definition is recorded in CAM.

1.15. ECAD - ODB++

① **ODB++**: Set default value for reading design from ODB++ file.



② **Select Unit to be Saved**: Select unit.

③ **Import from**: Select file type.
Compressed File: Compressed file type.
Data Folder: Folder type after decompressed.

④ **Select Step**
All: Read all design data
Selected Step(Including Sub-Board): Read only selected step design data

⑤ **Use Multiple Threads**: PollEx can support multi-treads when import file. Default is off mode.
Write Log File: Select this option to write a log history into *.log file.
Use the Origin point of the selected Step data: When this option is checked, use the origin point of the design data.
Skip Reading in Miscellaneous Data: Except to import Miscellaneous Data.
Separate Step Layers: Adding a step name at the end of the layer name when the design has step data.
User-defined Layer other than Default Layers: Read user defined layer file that defined layers to include or exclude.
Reload Layer Data(Applicable Only for Non-Intelligent data): This option is only applied to Legacy 32bit version. When the 32bit program cannot read big ODB++ data, this option creates a separate file per each layer.
Convert Drill to VIA: If Via hole describe in Drill layer, select this option to convert Drill to Via.
Add the Sub-board to specific Polygon Layer when Importing Panel data: When reading the upper level of ODB Step structure and including sub board, polygon is generated

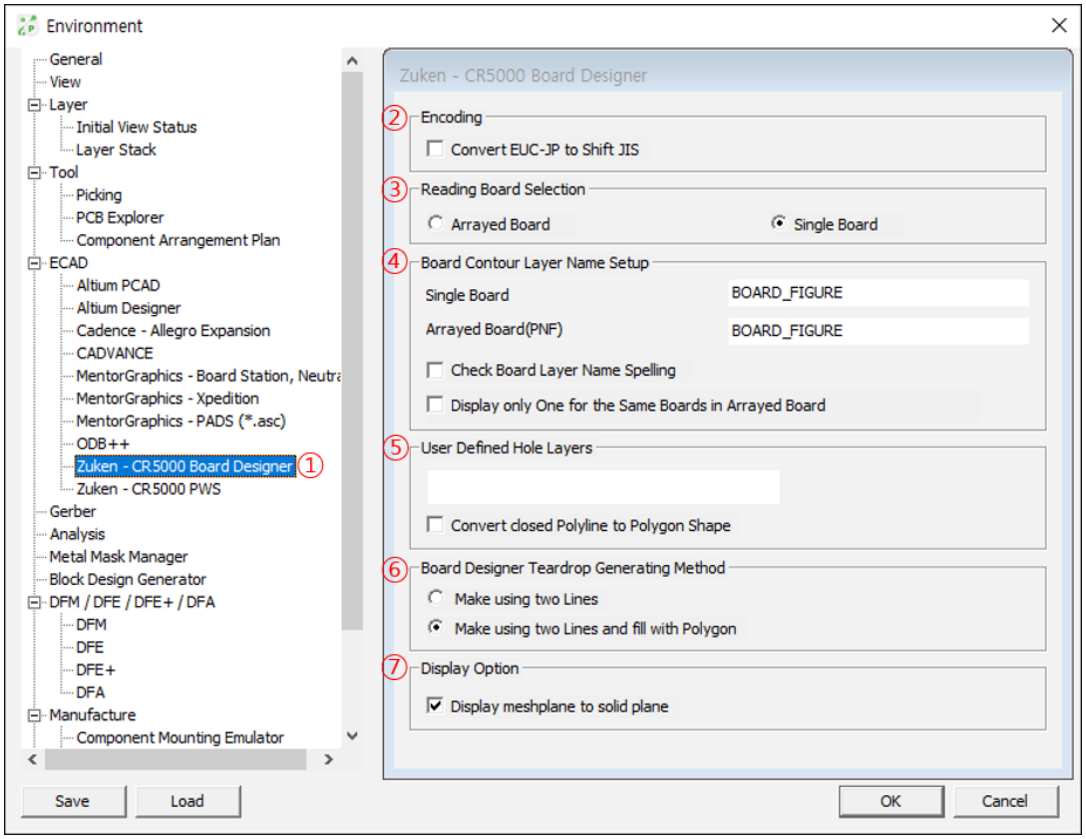
by sub board outline shape.

Property title used for Pin Pad: The objects which have a same property are combined as one pad shape. (ex.".geometry")

Property title used for Route Pattern: The objects which have a same property are combined as one net. (ex.".net_name")

1.16. ECAD - Zuken CR5000 Board Designer

① **Zuken CR5000 Board Designer**: Set the default reading parameters for Zuken CR5000 Board-Designer design.



② **Encoding**: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

③ **Reading Board Selection**

Array Board: Check this option to read arrayed board. PollEx PCB will read `*.pnf` and `*.ftf` file.

Single Board: Check this option to read single board. PollEx PCB will read `*.pcf` and `*.ftf` file.

④ **Board Contour Layer Name Setup:** Set here the board contour layer name for single and arrayed board.

Check Board Layer Name Spelling: When this option is checked, PollEx PCB will check the specified name and if there is no matching layer, show the warning message to users.

Display only One for the Same Boards in Arrayed Board: When user imports arrayed board and if there are same type board, PollEx PCB will shows only one board shape for multiple board.

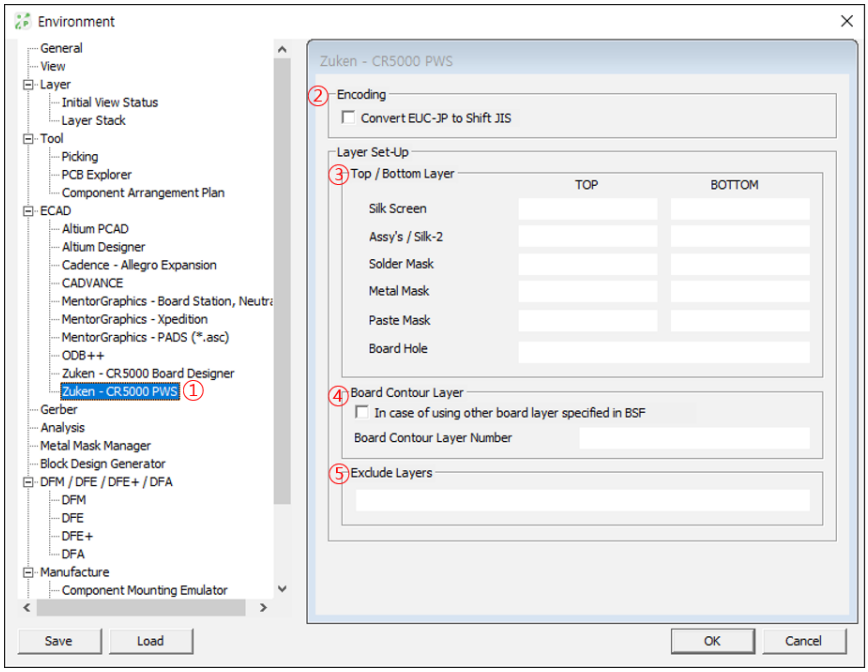
⑤ **User Defined Hole Layers**: When user used different name of hole layer, specify the layer name here.

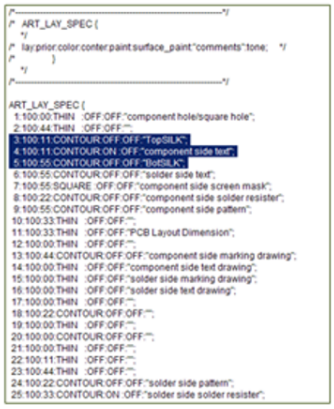
⑥ **Board Designer Teardrop Generating Method**: There is not defined for tear drop shape in Zuken Board Designer's ASCII file because we have to create tear drop shape based on user selection. Select either **Make using two Lines** or **Make using Lines and fill with Polygon**.

⑦ **Display Option**: When this option is checked, after importing design, show meshed plane shape with same as solid plane.

1.17. ECAD - Zuken CR5000 PWS

① **Zuken CR5000 PWS:** Set the default reading parameters for Zuken CR5000 PWS.





② **Encoding**: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

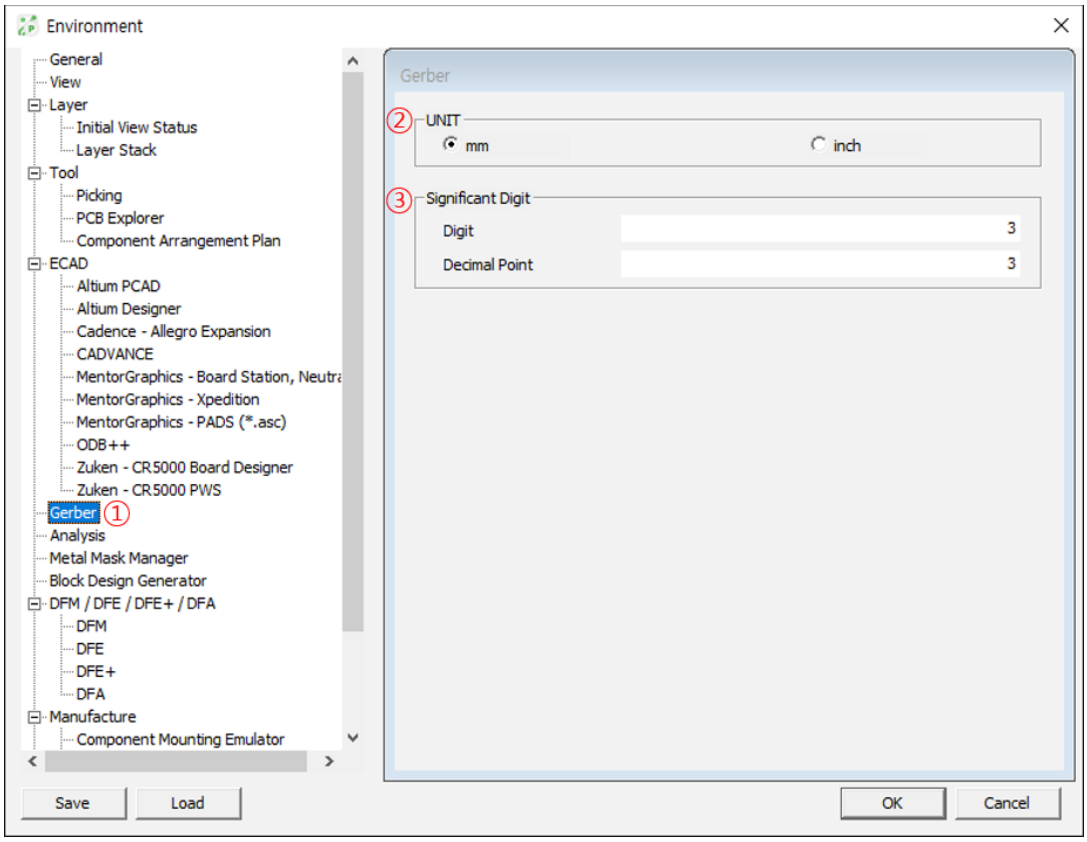
③ **Layer Setup**: Use this setting to read layer definitions into PollEx PCB design. Zuken PWS designs may have different layer settings depending on users and depending on manufacturing process. To complete this task, refer the BSF(Board Specification File) file used in PWS.

④ **Board Contour Layer**: Specify the board contour layer name, in case of using board contour layer differently than that is used in BSF.

⑤ **Exclude Layers**: Exclude specified layers.

1.18. ECAD - Gerber

① **Gerber**: Set the default reading parameters for GERBER file.



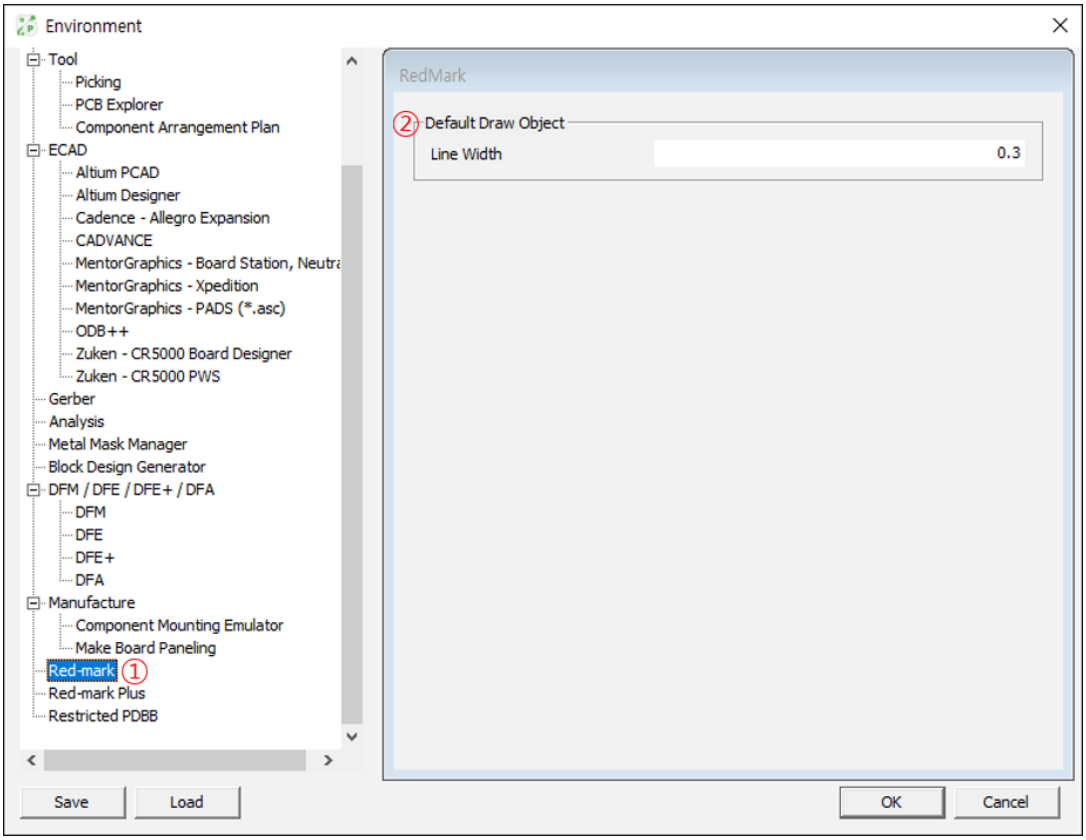
② **UNIT**: Set the unit of GERBER file.

③ **Significant Digit**: Set the decimal point and effective number of characters for numbers. **DIGIT** means real part of number and **DECIMAL** means parts behind ".”(dot). Some of GERBER file's representation would be 00235.567. In this case, **DIGIT** value would be 5 and **DECIMAL** would be 3. Generally, PollEx PCB ignores the value of **DIGIT**.

1.19. Redmark

① **Redmark:** Menu for setting Redmark's environment.

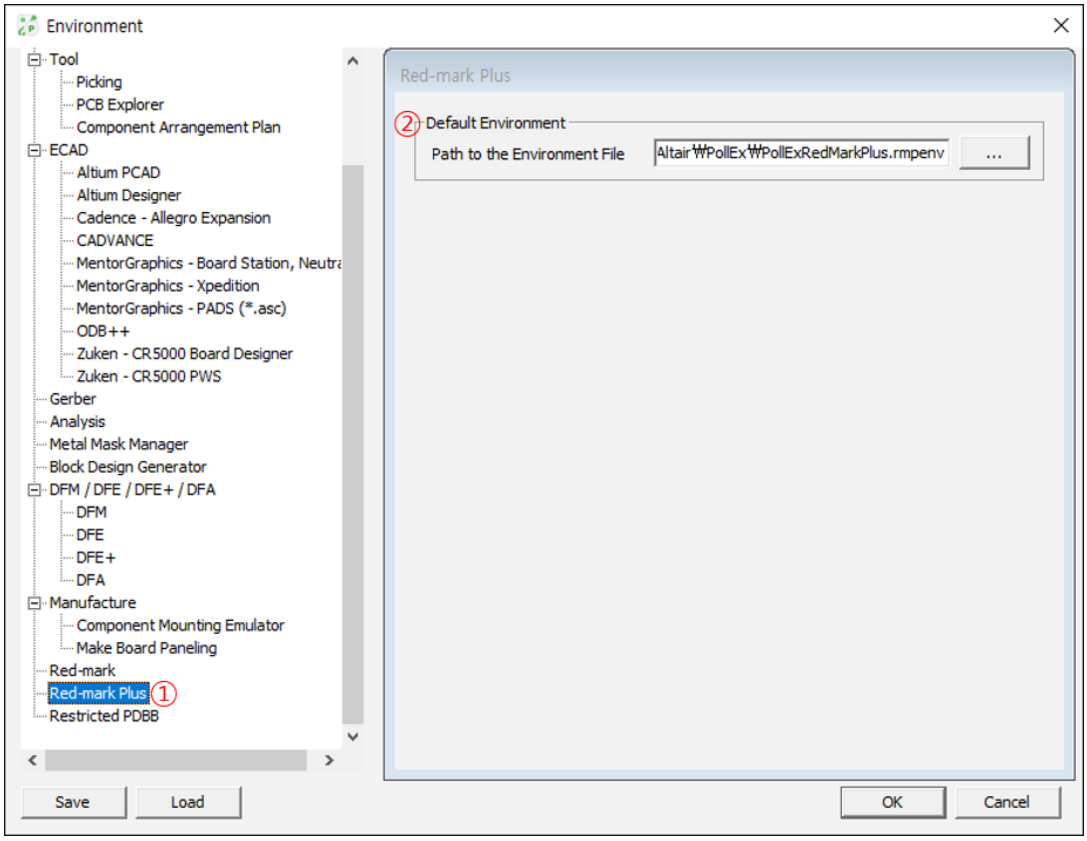
② **Default Draw Object**: Can set default line with of drawing object.



1.20. Red-mark Plus

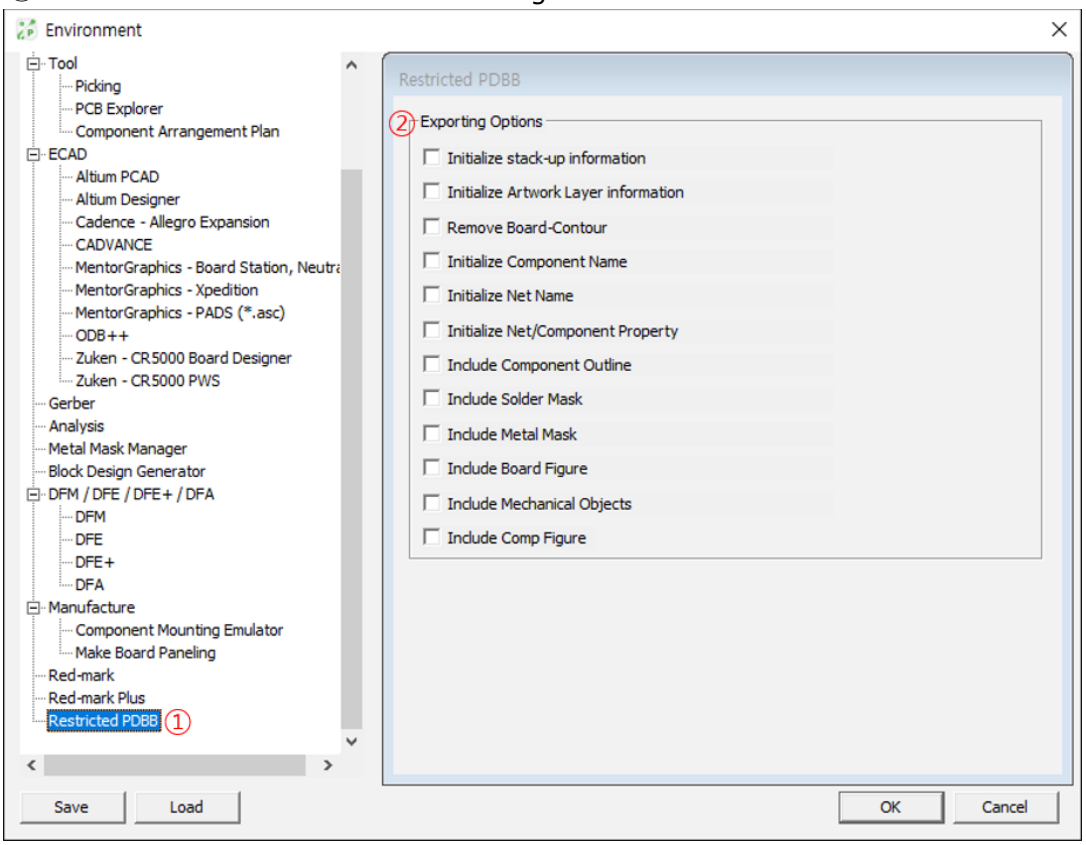
① **Red-mark Plus**: Menu for setting Red-mark Plus environment.

② **Default to the Environment File**: Can set default Environment File Path.



1.21. Restricted PDBB

① **Restricted PDBB**: Menu for setting Restricted PDBB's environment.



② **Exporting Options**

Initialize stack-up information: Reset stack-up information and make it with default value.

Initialize Artwork Layer information: Reset artwork layer information and make it with default value.

Remove Board-Contour: Remove board contour data and make it with basic rectangle geometries.

Initialize Component Name: Remove all part's name information and rename them with string starting "PartXXX". All other footprint, package and device name will be re-arranged. Vias and padstacks name will be re-arranged also.

Initialize Net Name: Remove all nets' name and rename them with string starting "NetXXX". Vias and padstacks name will be re-arranged also.

Initialize Net/Component Property: Remove all properties assigned to net and components (reference designator).

Include Component Outline: Include all component outline of component(Artwork Layer-201: COC Top, 202: COC Bottom).

Include Solder Mask: Include all solder mask layer.

Include Metal Mask: Include all metal mask layers.

Include Board Figure: Include all board figures.

Include Mechanical Objects: Include all mechanical objects.

Include Comp Figure: Include all Component Figure Data.

2. Layer

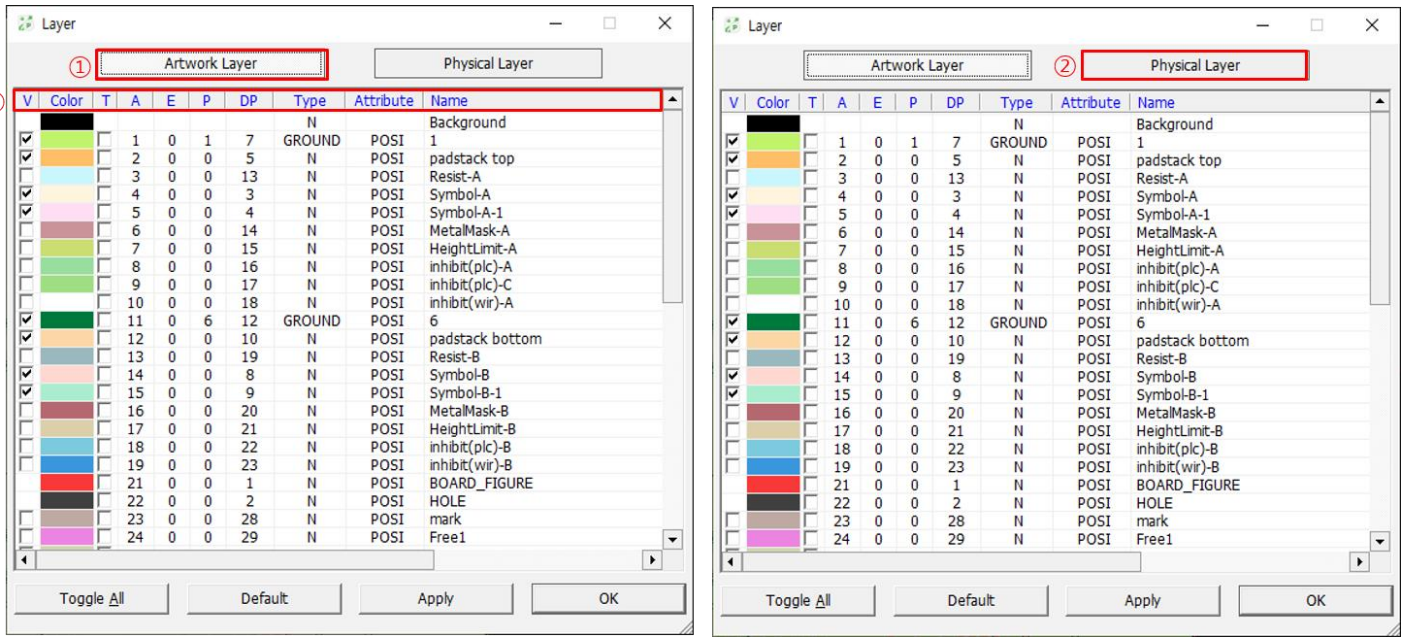
PollEx PCB has two terms to call layers, artwork and physical layer. Physical layer means the physical stack-up layer whereas artwork layer means layer used in ECAD tools. Especially, PollEx PCB has another order of artwork layer. It means artwork layers in PDB have specific purpose depending on index of layers. Following table show the layer's usages in PollEx PCB.

Detail descriptions are followings,

Lay No	Usage	Comment
1	Top	
2	Top Pad	For component's top
3	Top Solder Resist	
4	Top Silk	
5	Top Silk Text	
6	Top Metal Mask	
7~10	Top reserved	
11	Bottom	
12	Bottom Pad	For component's bottom
13	Bottom Solder Resist	
14	Bottom Silk	
15	Bottom Silk Text	
16	Bottom Metal Mask	
17~20	Bottom reserved	
21	Board Contour Layer	
22	Drill Layer	
23~80	Board Figure Geometries	
81~200	Inner Layer	
201	Top Component Outline	For component's top
201~210	Top reserved	
211	Bottom Component Geometries	For component's bottom
211~220	Bottom reserved	
221~400	Gerber Layer	
401~450	Top reserved	For Component's top
451~500	Bottom reserved	For Component's bottom
551~	Board Figure Geometries	

2.1. Layer

To control or set the layer status, use the menu, **Setting > Layer**. (Shortcut key: ***Alt + L***)

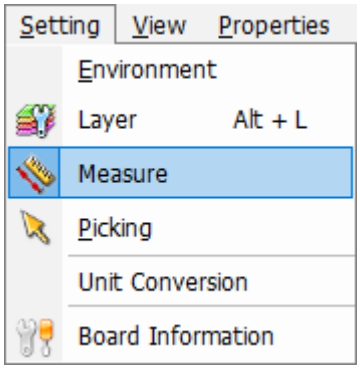


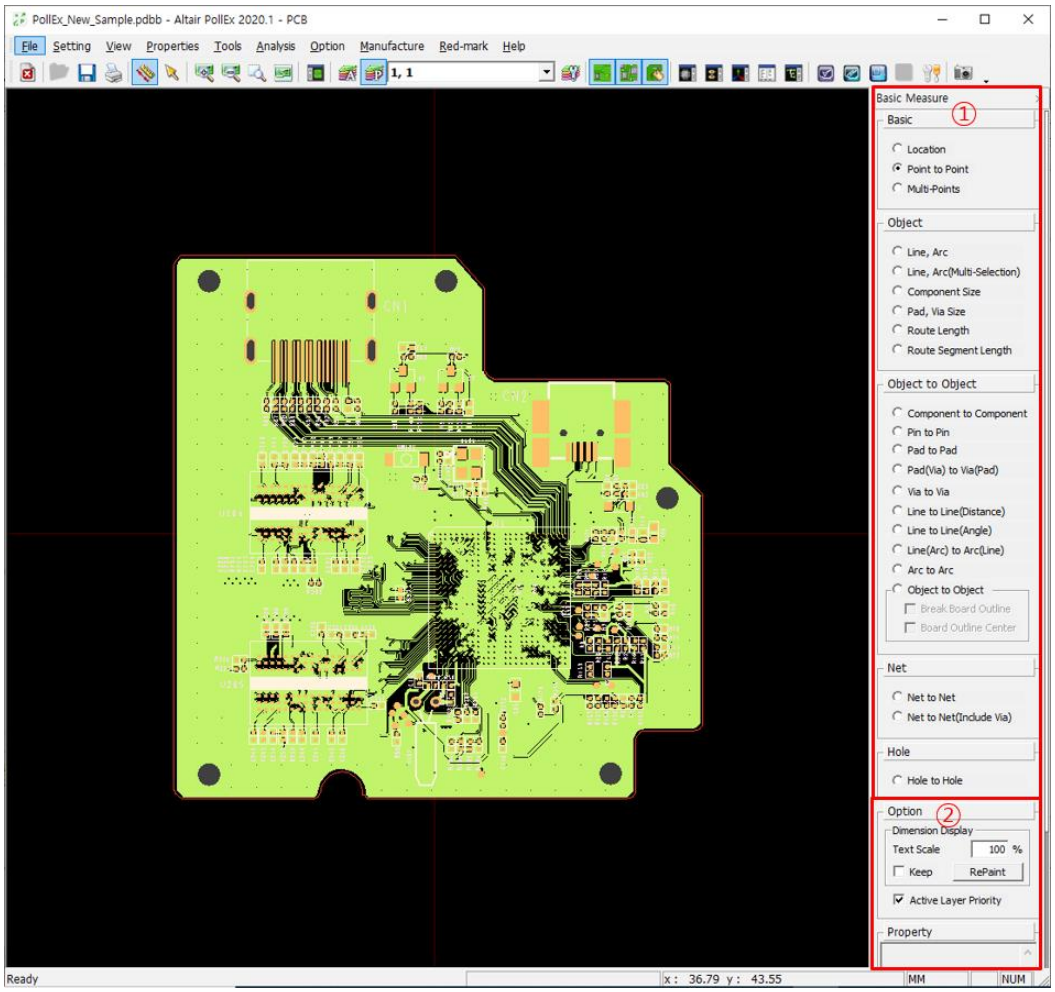
① **Artwork Layer**: Select this button to show layer orders with artwork layers.
② **Physical Layer**: Select this button to show layer orders with physical layers.
③ Each column's abbreviation means properties of layers.
V: Make visible On/Off for layer.
T: Make transparent layer status.
A: PollEx PCB's artwork layer number.
E: ECAD artwork layer number.
P: Physical layer number.
DP: Display Priority for showing layer. Lower number layer will be displayed at top.
Type: Physical layers' type.
Attr: Layer attributes. Values will be one of positive or negative
Name: Layer name.
With layer control window, user can do work for selecting layer, making layer status visible/invisible.

④ At layer type selection, select one between artwork and physical layer.
⑤ Among layer list, select one of layers.
⑥ Launch **Layer** window for detail set-up for layer status.

3. **Measure**

Measure tool is a function to measure the size or dimension of objects. Use the menu, **Setting > Measure**.





After launching measure tool, user can see above dialog window at right sides in main window.

① Select measuring type and object to measure.

② Measuring results will be displayed at property window. Text displaying ratio on screen is set as 100%. However, user can change the text scale if the showing text size is small and user wants to increase the size. **Keep** button maintain this ratio until the window is closed.

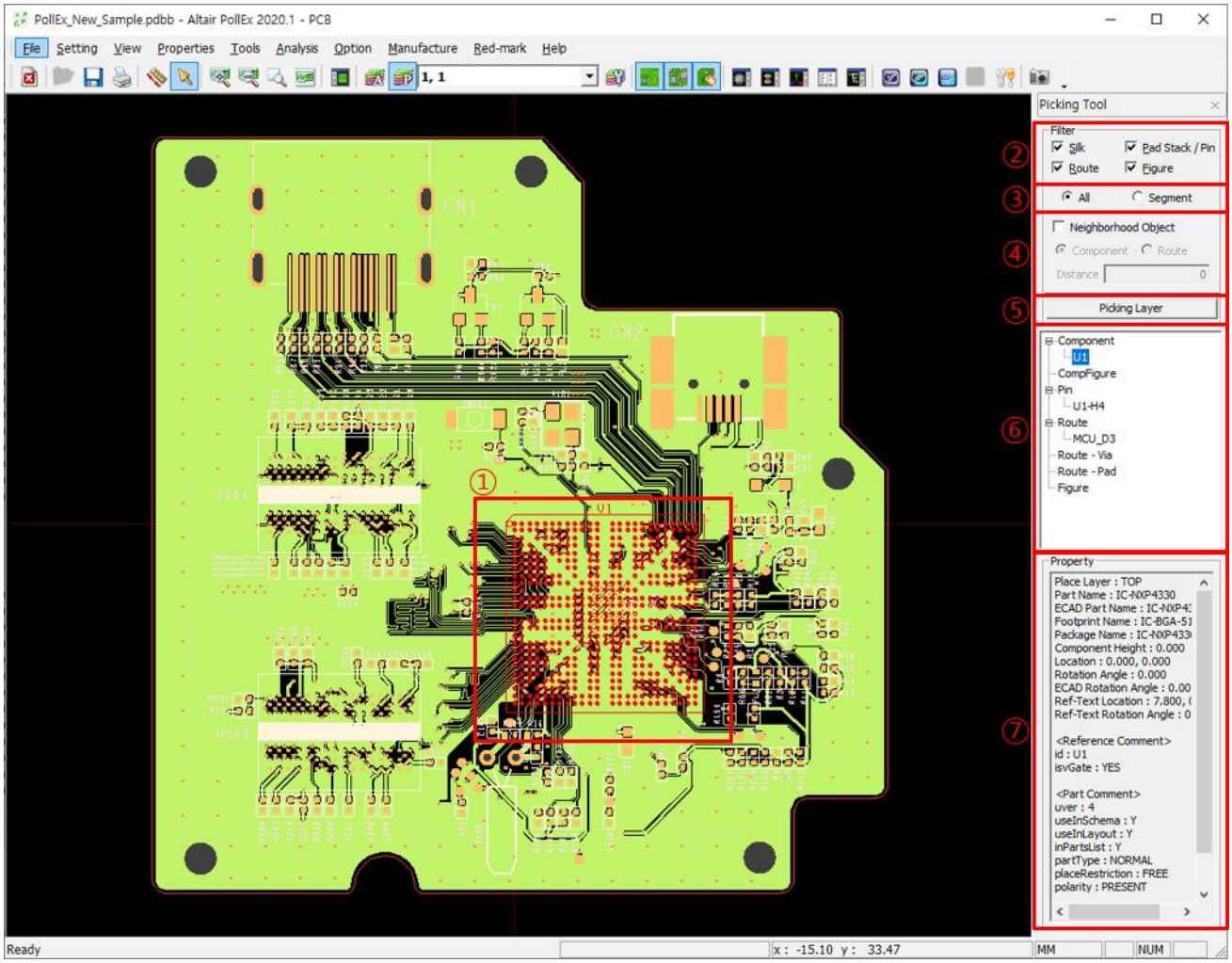
Upon using following proper function, user can easily check the size or distance between objects.

- **Point to Point**: Measure the distance between two points.
- **Line, Arc**: Measure line or arc's segment length.
- **Route Length**: Measure total net length.

- **Route Segment Length**: Measure selected segment length in routing net.
- **Comp to Comp Dist**: Measure center to center for components.
- **Pad(Via) to Via(Pad)**: Measure pad(via) to another pad(via).
- **Object to Object**: Measure object to object.

4. Picking

This is the tool for checking the properties of certain objects on board by mouse picking. Use the menu, **Setting > Picking**.

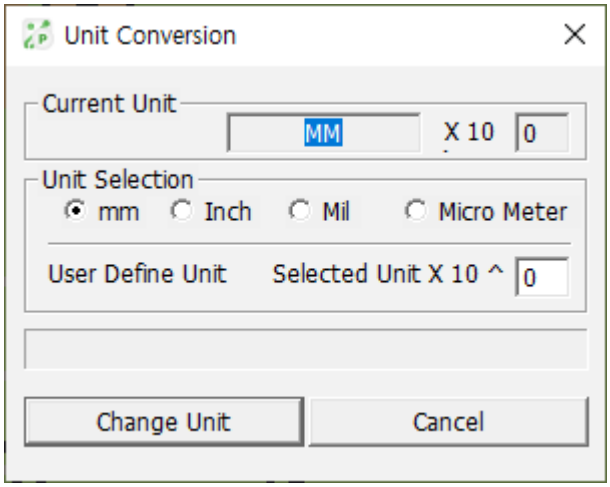


After launching picking tool, **Picking Tool** dialog box will be shown at right-side on the screen. Upon selecting object(①)**,** selected objects properties or information will be shown on tab(⑥and⑦**)** window. Especially, at tab window ⑥, PollEx PCB shows board's hierarchical structure for selected objects. At window tab ⑦, all related object's properties will be shown. Followings are each tab's name and usages.

① Picked object on screen.
② **Filter**: Filter for selecting target objects.
③ Selection either **All** or **Segment** for routing net.
④ **Neighborhood Object**: Select object in given area for routing net or component.
⑤ **Picking Layer**: Select layers which users want to select. Default is all layers.
⑥ Selected object listing window.
⑦ Property tab to show selected objects' properties.

5. **Unit Conversion**

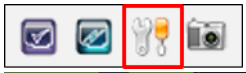
Basically, PollEx PCB uses the unit from ECAD design. But user can change the unit of design. To do this, use the menu, **Setting > Unit Conversion**.

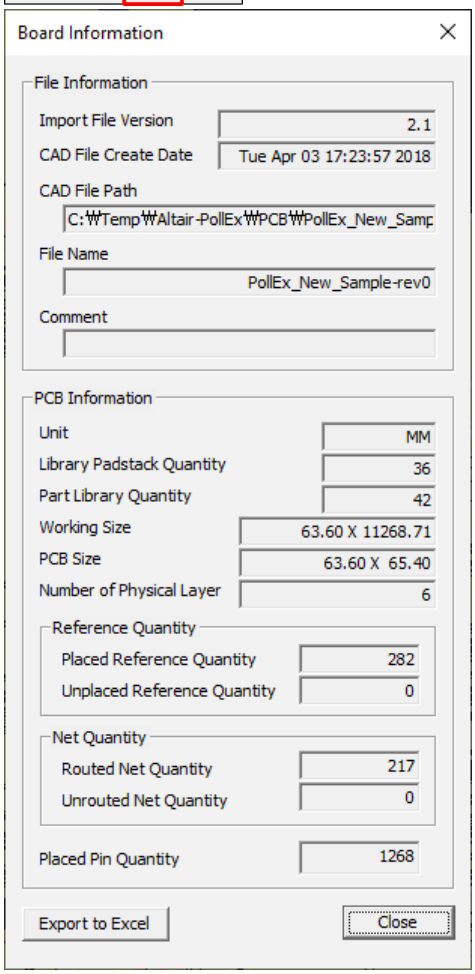


PollEx PCB supports 4 different units, mm, Inch, Mil and Micrometer. Select target unit and press **Change Unit** button to complete changing unit.

6. **Board Information**

Board Information menu shows all information for design. Use the menu, **Setting > Board Information**.





User can check the board creation date, file path, unit, board size, number of components on board, number of nets, and other information.

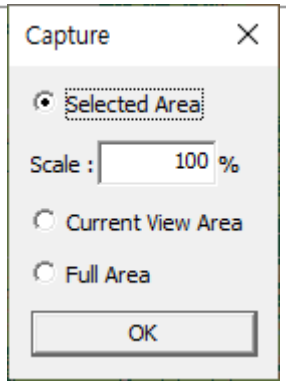
View

User can use **View** menu to control display more efficiently.

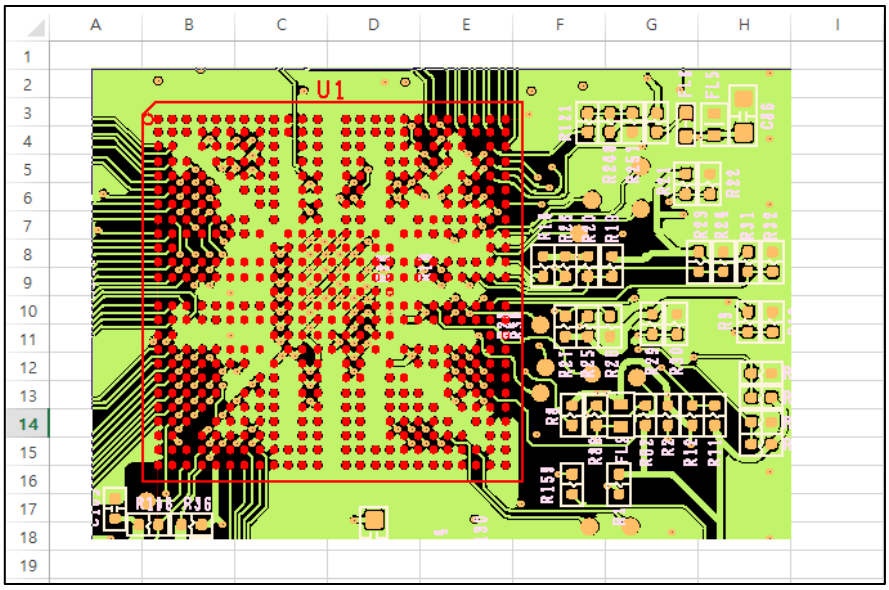
① Zoom In/Out/Window/Zoom 1:1 Toggle 1:1: use the menu to control view status.
② Set Capture Window: Screen capture option.
③ Mirror View/Board Rotation: make mirror for board's image or rotate board.
④ Route/Component On/Off, Polygon Fill/Unfill, Net Display On/Off: control the objects' viewing status on board.
⑤ Board Mini-Map: show small map with which user can see whole board and working area.
⑥ Bar Menus.

1. **Set Capture Window**

Use this function to make partial image capture, screen capture, full area capture. Saved image will be saved in system buffer for using other Windows applications. Use the menu, **View > Set Capture Window**.



Fix the screen and press the above menu button. Next, select two points on screen with mouse click to set rectangle area. Then pressing the key **Ctrl + C** will save image into system buffer. To use system buffer image, use the key **Ctrl + V**.

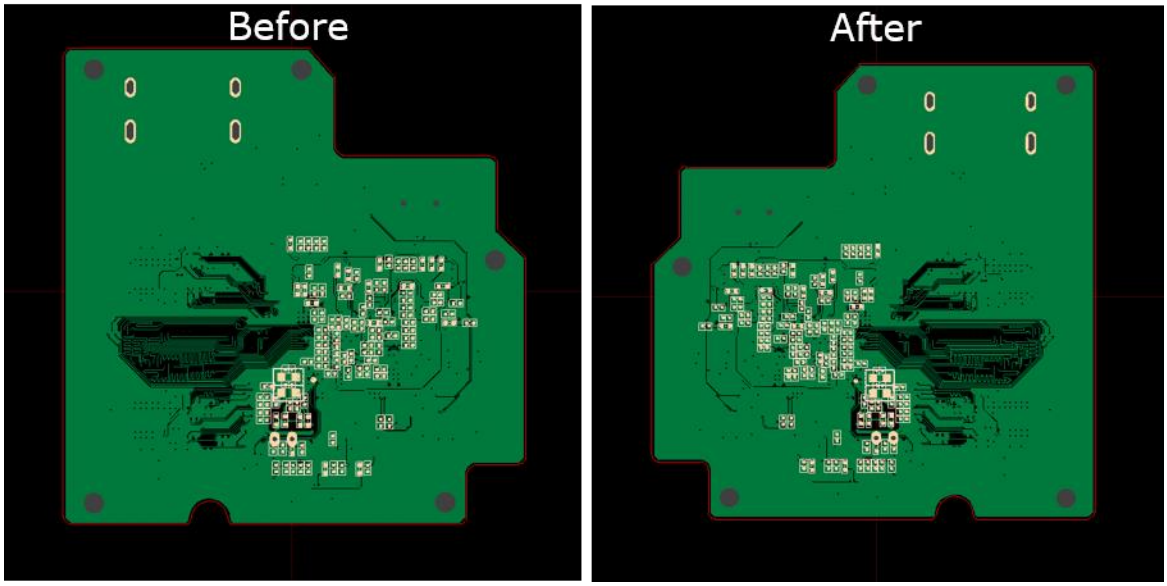


2. **Mirror View / Board Rotation**

User can see the mirrored board image with **Mirror View** menu. Also, user can see the rotated board using **Board Rotation** menu.

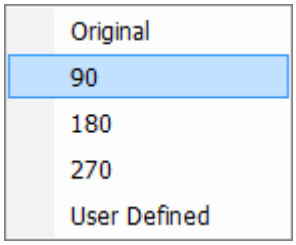
2.1. Mirror View

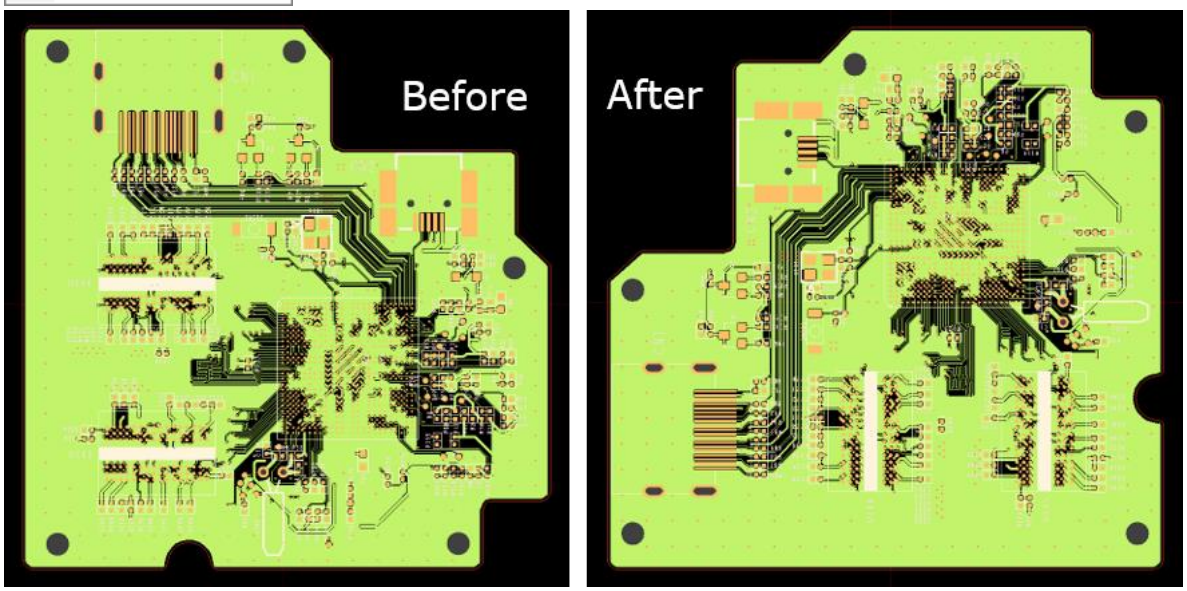
Use the menu, **View > Mirror View**. Many cases, user needs to see the bottom shape with mirrored status to compare to real PCB image.



2.2. Board Rotation

Use the menu, **View > Board Rotation**. PollEx PCB supports rotation angles for 90, 180, 270 and user defined angle.

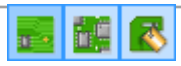


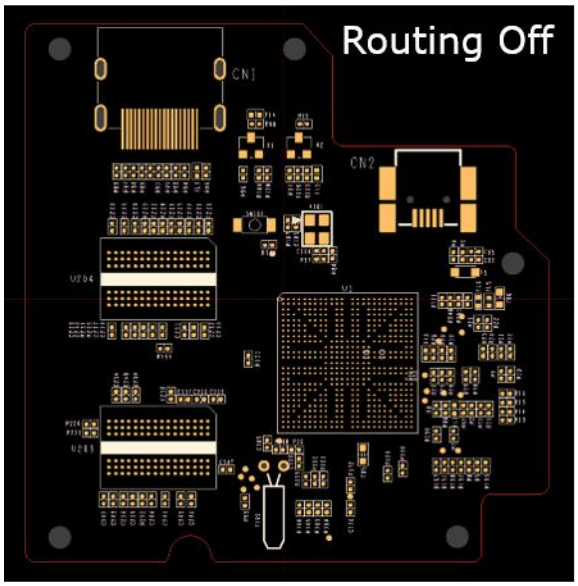


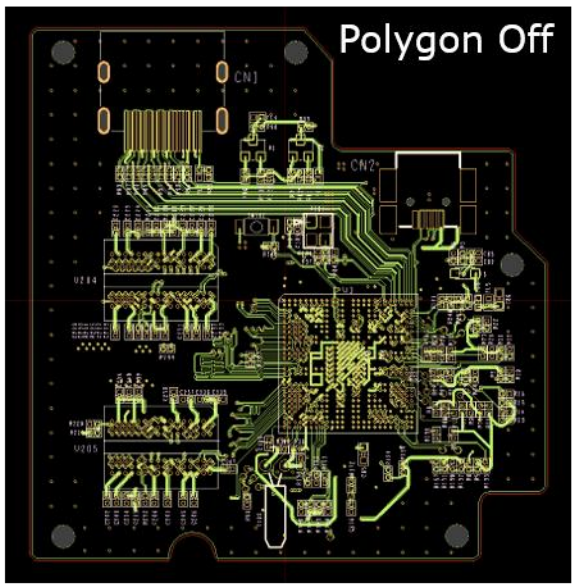
3. **Route on, off /Component on, off / Polygon Fill, Unfill**

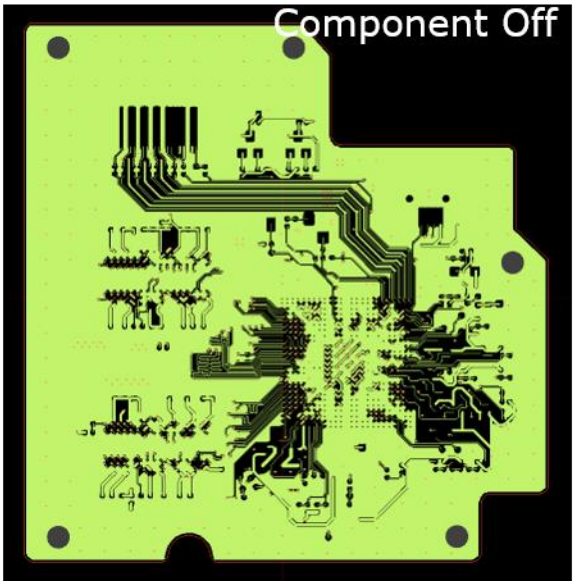
   To see components, routing pattern and copper pour more efficiently, use these menus. All below three menus are running with toggle mode.

   View > Route On/Off
   View > Component On/Off
   View > Polygon Fill/Unfill



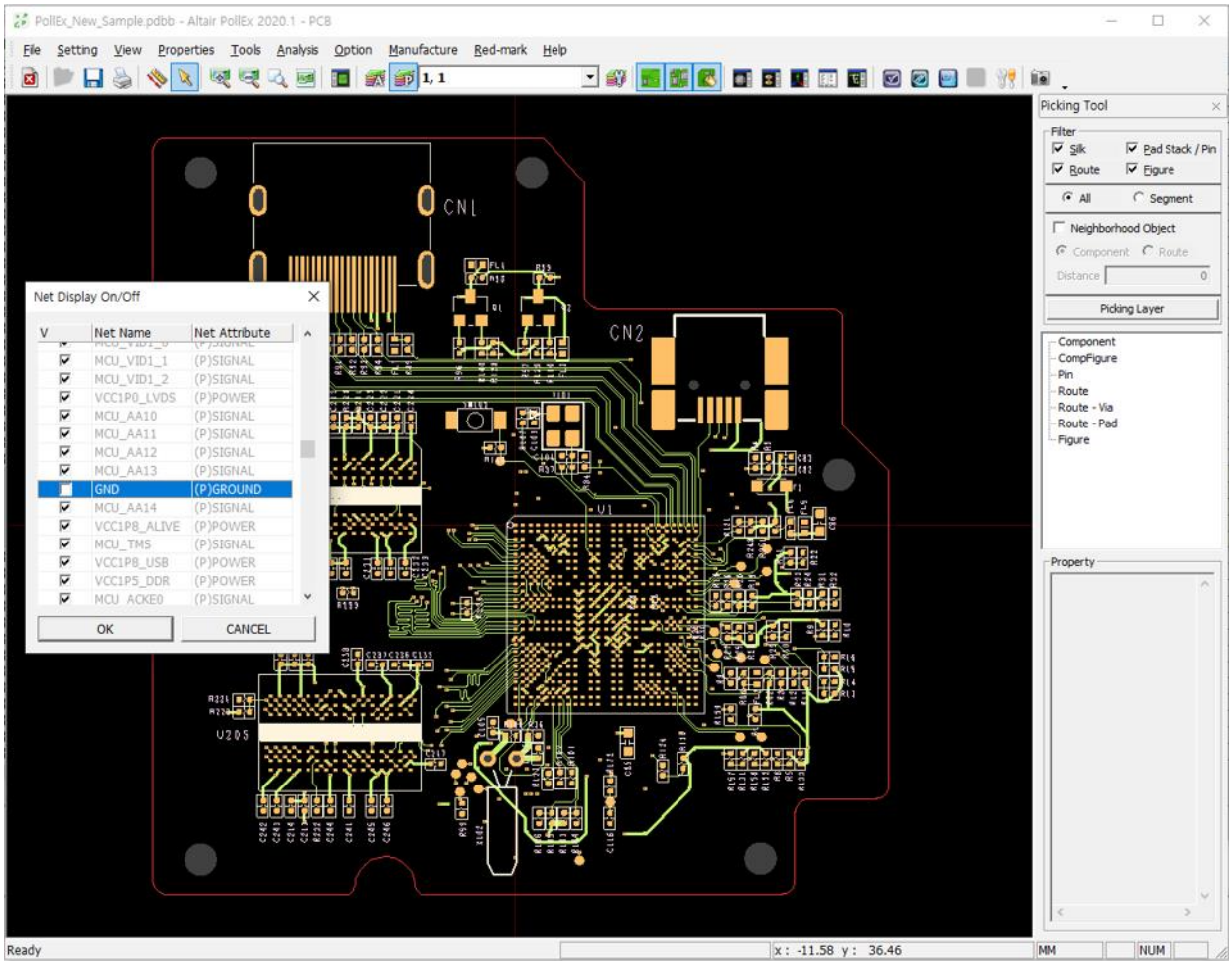

Routing Off


Polygon Off


Component Off

4. **Net Display On/Off**

PollEx PCB can display or turn off display for a certain net(s). Use the menu, **View > Net Display On/Off**.

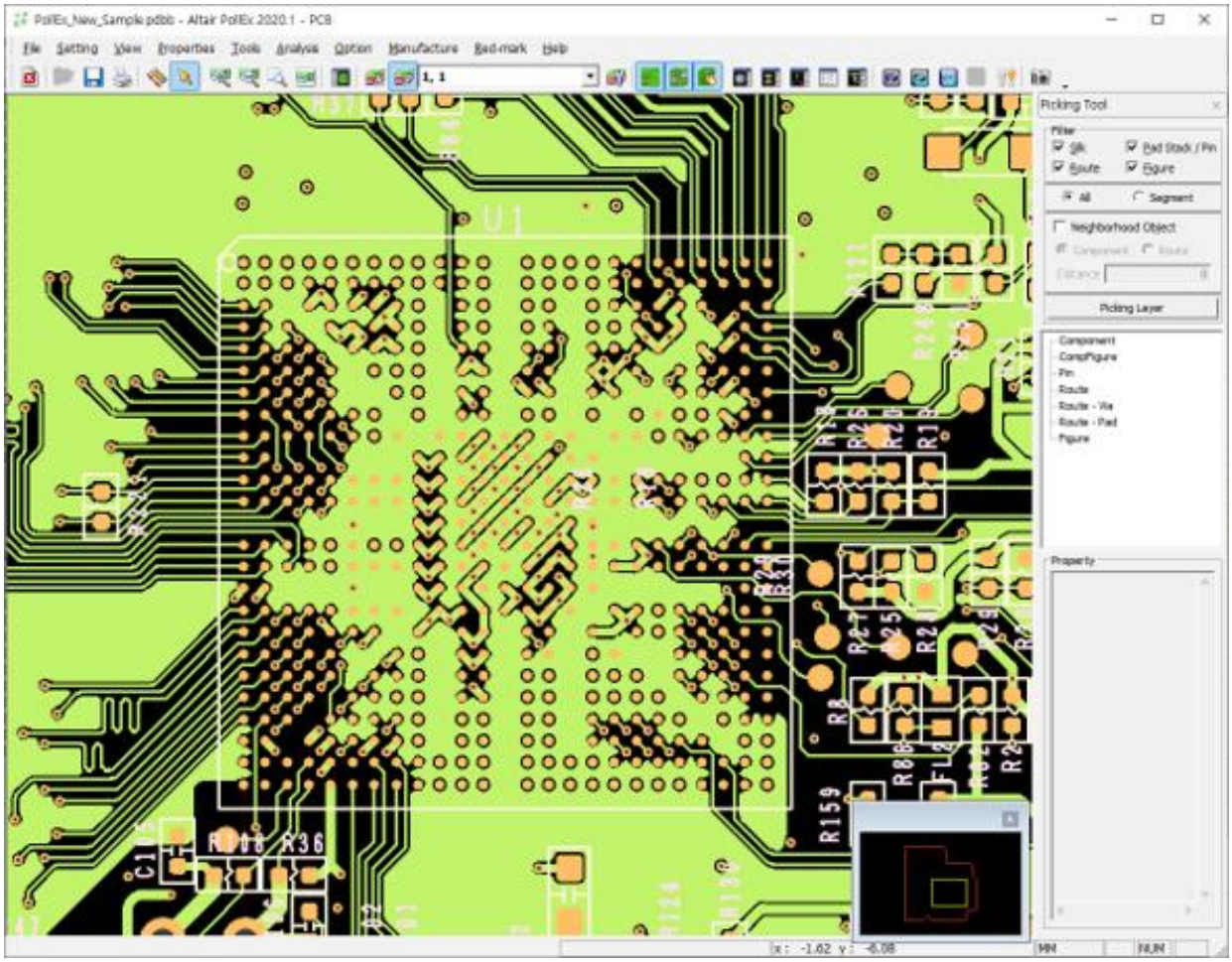


① Checking "V" column turn on and off for selected nets.

② After selecting nets, pressing **OK** button will apply changes to screen.

5. Board Mini-Map

While exploring PCB design, this function help user to check current location regarding to whole board and see the whole board image. Using the following menu to launch the min-map window, **View > Board Mini-Map**.



On mini-map, red line means the board contour.

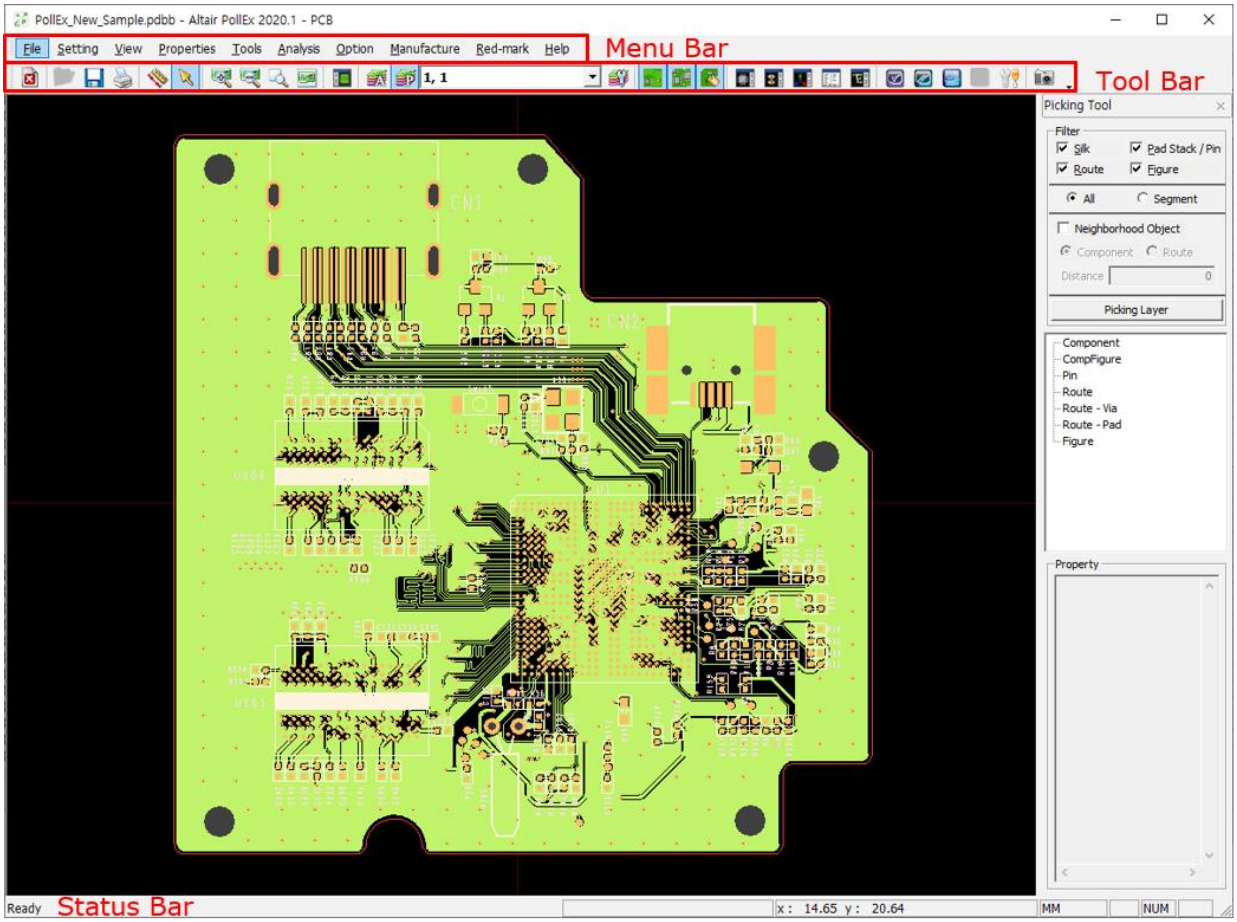
6. Menubar, Toolbar, Status bar

Menubar contains main menu list and tool bar contains icon menus and status bar show working status, respectively. User can hide each menu using following menus.

View > Menu bar

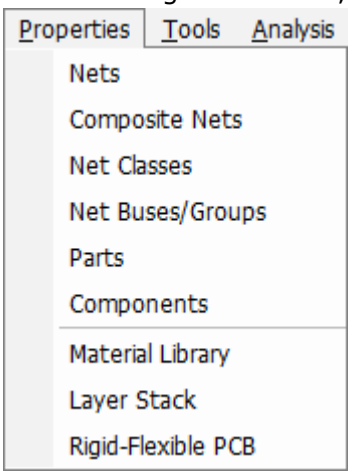
View > Tool bar

View > Status Bar



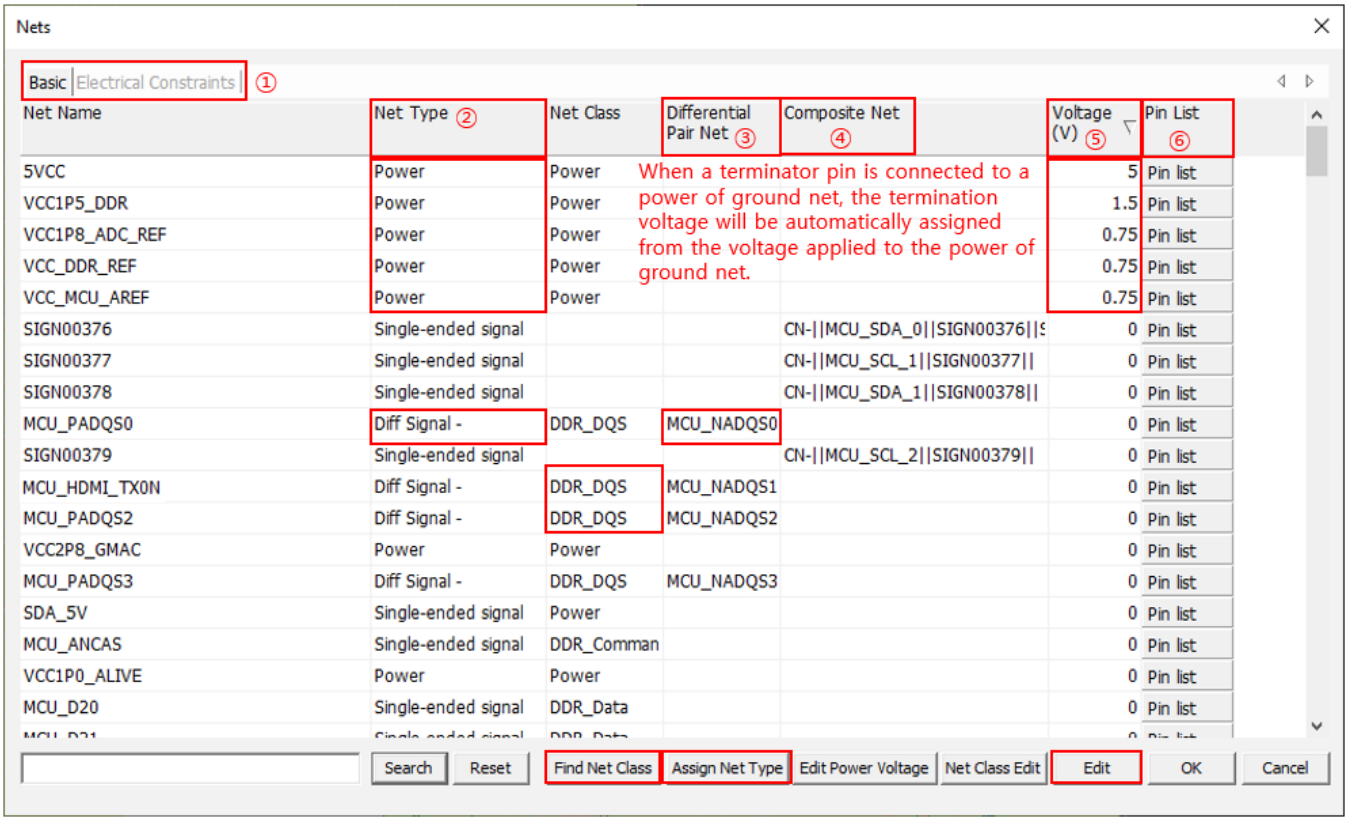
Properties

Properties menu has 5 different sub menus, **Nets**, **Composite Nets**, **Parts**, **Material Library** and **Layer Stack**. Using sub-menus, users can see and edit properties of objects on board or library link.



1. Nets

Net's properties are basic attributes influencing the electrical analysis. The voltages assigned to the Power/Ground net will be applied to the connected terminator pin as termination voltage. Net pairs defined as **Differential Signal Positive (+) & Negative (-)** will be recognized and simulated as differential pair by just assigning the driver model to one of both Positive (+) or Negative (-) net. ***Properties - Nets*** menu will invoke a dialog with default net properties as **Single-ended signal** for all nets included in the activated PCB system, by double clicking a net or selecting a net and clicking the ***Edit*** button, user can define or modify the ***Net Type***(②), ***Voltage***(⑤) and electrical constraints(①). By clicking the ***Pin list***(⑥), user can verify the list of all pins connected to the selected net.

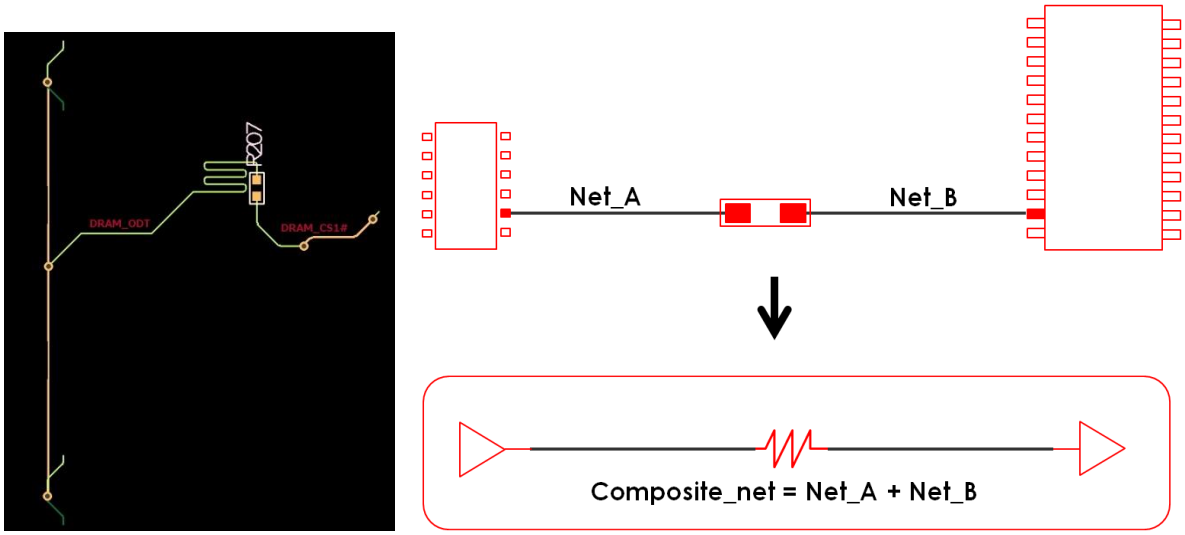


By clicking the ***Assign Net Type***, user can set net property automatically using net information which described in IBIS files and property.

By clicking the ***Find Net Class***, user can set net class automatically using pre-defined net class search string file.

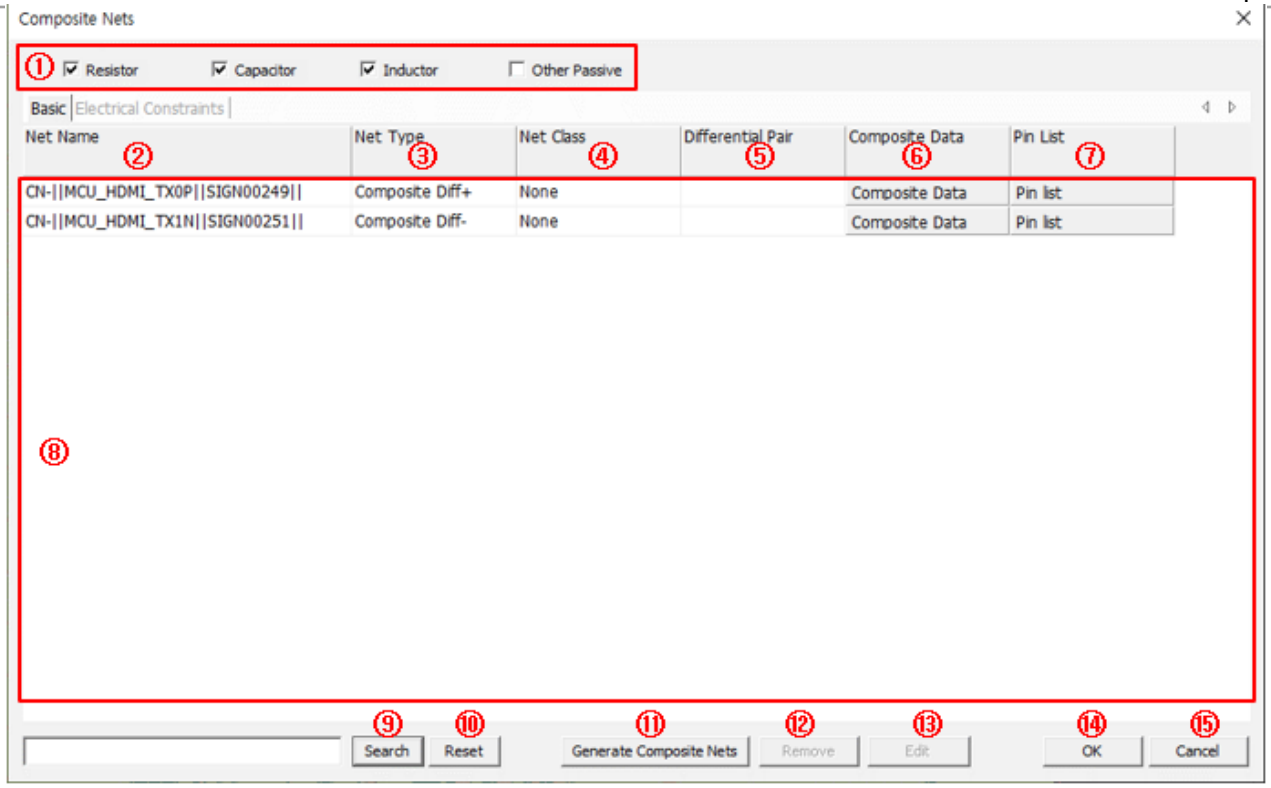
2. Composite-nets

When two or more nets are serially connected through passive components such as resistor, electrical analysis must be made for the entire signal path encompassing the multiple nets connected with these passive components. These nets are modeled as composite nets in PollEx PCB environment. The composite nets are automatically generated by PollEx PCB which references the schematic data to configure it by checking the connectivity of the selected passive components to each net.



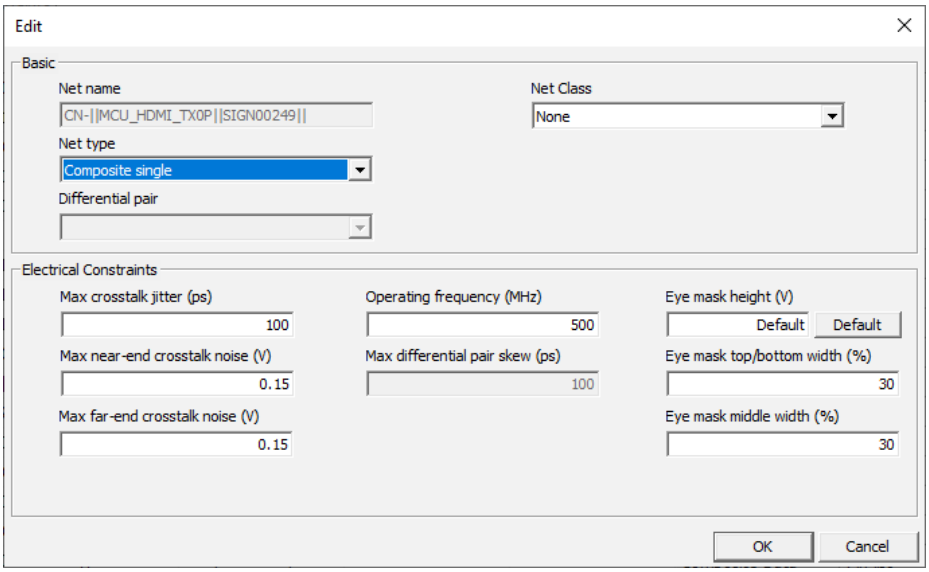
In the upper left figure, two nets are connected with the **R207** resistor, without composite nets operation, these two nets might have **open** terminal for each then electrical simulation results for the nets wouldn't be appropriate.

Properties - Composite Nets menu provides versatile ways to manipulate the **Composite Nets** generation and manage features with many options and operations illustrated below.

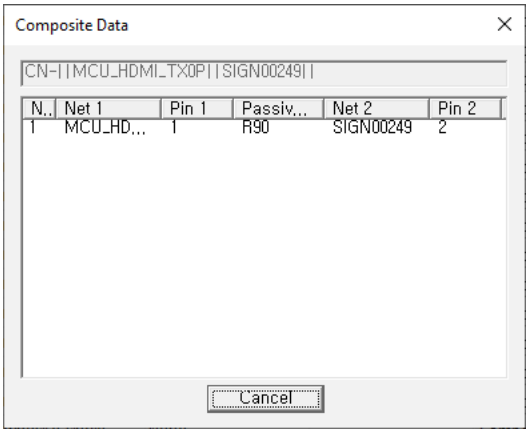


In **Composite Component Area**①, user can select components to be used to generate composite net. Two nets connected with this component are modeled as composite nets.
After selecting composite component, upon clicking ***Generate Composite Nets***⑪ button, the list of composite nets will be displayed on **composite net result display region**⑧.

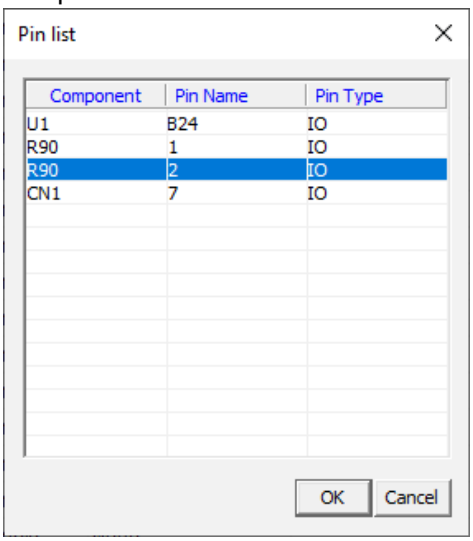
User can remove or edit composite net result by **Remove**⑫ or **Edit**⑬ button.
By double clicking one of composite net, the Edit dialog will be displayed. User can change **Net Type**, **Net Class** and **Electrical Constraints**.



By clicking **Composite Data**(6) field, user can review the composite net connection structure.



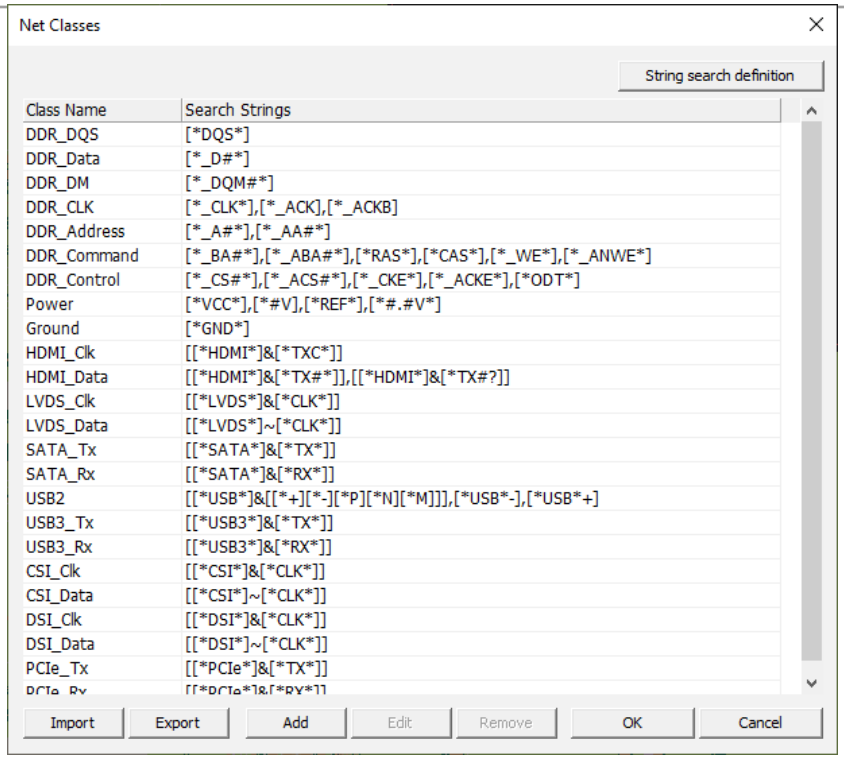
By clicking **Pin List**⑦ field, user can review the component and pin number connected to this composite net.



3. Net Classes

User can classify nets according to their electrical characteristics. By using net class assigned to each net, DDR nets are automatically grouped when performing **Automatic DDR Bus Analysis**.

Upon selecting **Properties-Net Classes** menu, a default net class, string filter, is displayed as shown below.



User save and re-load net class file using **Import** and **Export** button. User can edit current net class item using **EDIT** button, add a new net class item using **Add** button.

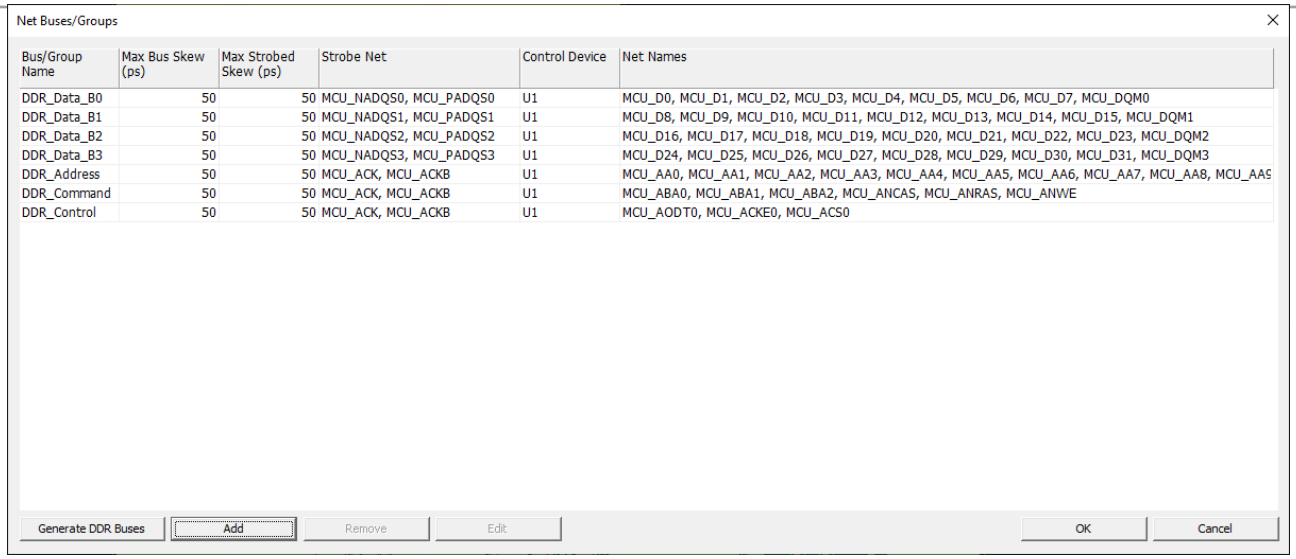
Upon clicking ***Add*** button, the **Net Classes** dialog will be open. User can assign new **net class name** and **search strings**. Two operators are used in the search string: # and *.
*: Any string
#: One Number

This net class definition will be used at **Properties-Nets** menu to assign net class to each net. By using net class assigned to each net, DDR nets are automatically grouped when performing **Automatic DDR Bus Analysis**.

4. Net Buses/Groups

User can generate Net Group or Bus Group using this menu. This will be used for PollEx DFE+ option. User can classify nets according to their electrical characteristics. By using net class assigned to each net, DDR nets are automatically grouped when performing **Automatic DDR Bus Analysis**.

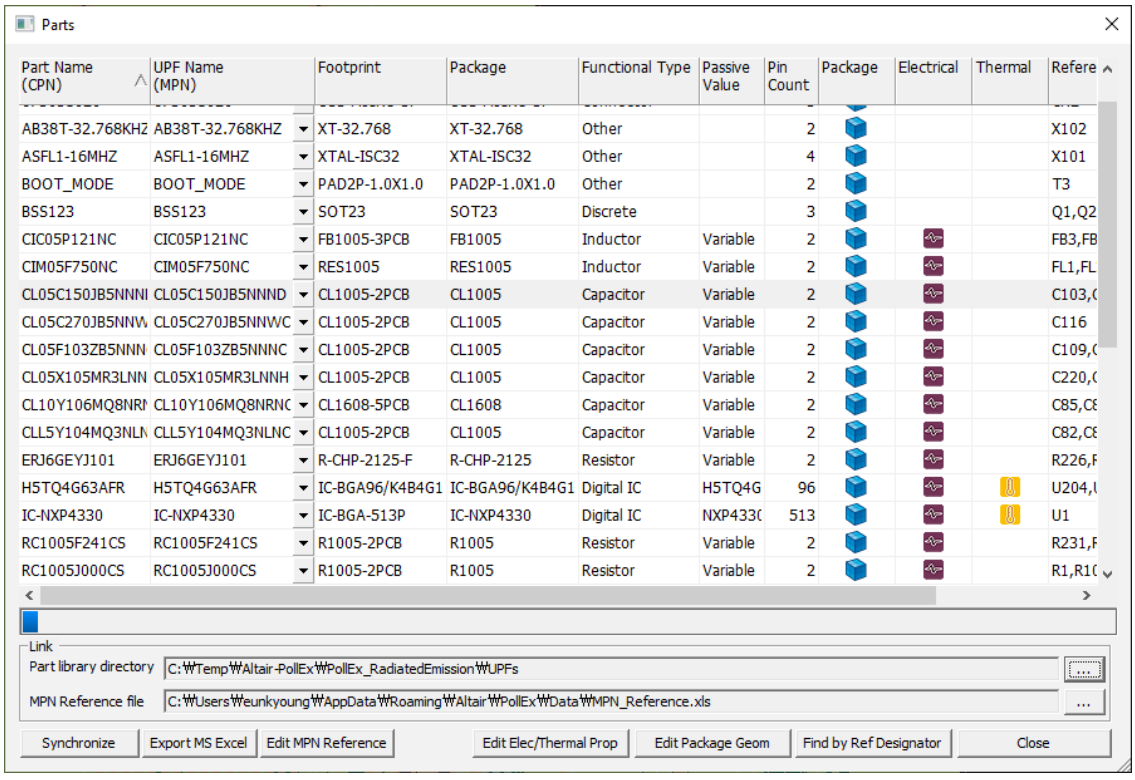
Upon selecting ***Properties-Net Buses/Groups*** menu, the Net Buses/Groups dialog will be open. Just clicking ***Generate DDR Buses*** button, the DDR Bus groups will be generated automatically. In this process, it creates a following table by referring to **Net Classes** and **Electrical constraints** of nets.
User can add arbitrary bus group using ***Add*** button.



5. Parts

Show the parts information. Use the menu, **Properties > Parts**.

Parts menu show the status of the properties assignment to the parts which are included in the current PCB system to analyze. The unified parts created by PollEx UPE (Unified Part Editor) can have versatile information such as electrical buffer model, package thermal parameters and 3D package geometry which needed for electrical, thermal and 2D/3D assembly analysis (by **PollEx DFA** and **PCB assembly viewer**) and it would be stored in specific folders in local or server system.

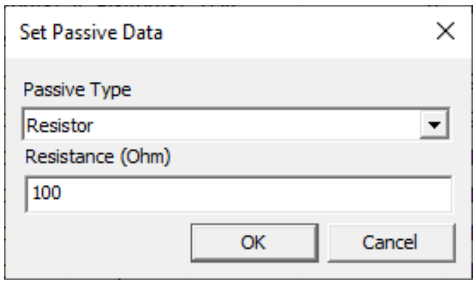


6. Components

Components menu lists all components (reference designators or location identifiers) in current design. In this menu users can assign different RLC value to each different

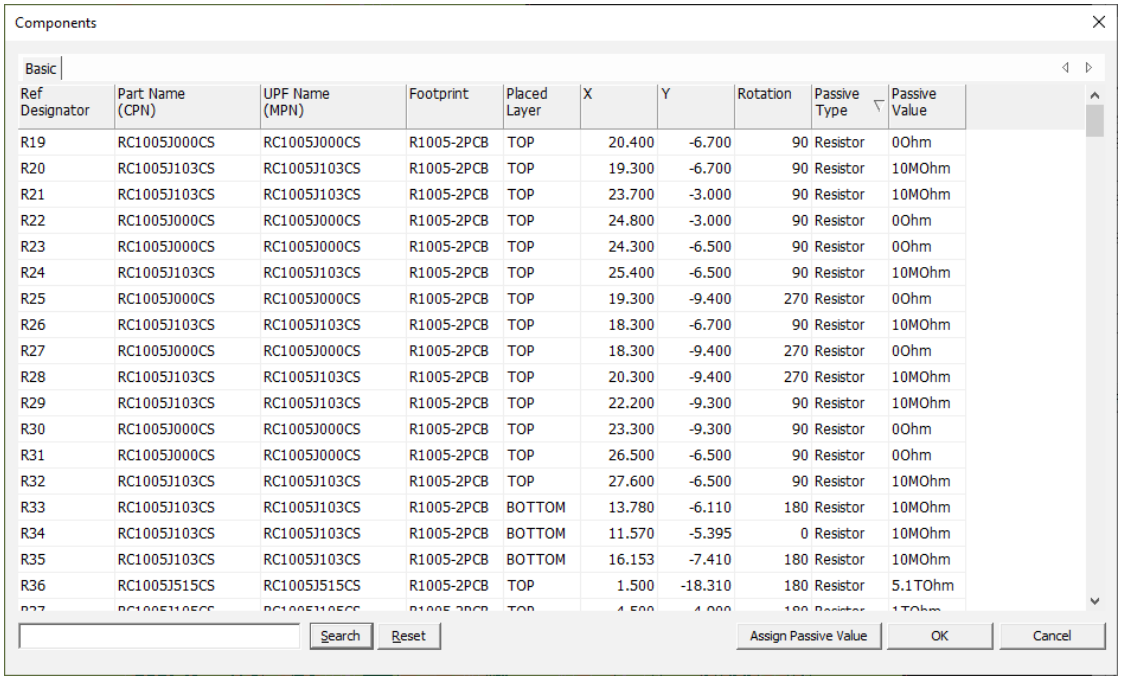
Normally, PollEx SI assigns the same RLC value for the passive component has a same part name. In this menu users can assign different RLC value for the passive component has different reference designator number.

Upon double clicking the passive component, the **Set Passive Data** dialog will be open.



Then user can select ***Passive Type*** and enter the ***Resistance***.

Upon clicking ***Find Passive Component Value*** button, user can assign all the passive component's **Type** and **Value** automatically.



Ref Designator	Part Name (CPN)	UPF Name (MPN)	Footprint	Placed Layer	X	Y	Rotation	Passive Type	Passive Value
R19	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	20.400	-6.700	90	Resistor	0Ohm
R20	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	19.300	-6.700	90	Resistor	10MOhm
R21	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	23.700	-3.000	90	Resistor	10MOhm
R22	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	24.800	-3.000	90	Resistor	0Ohm
R23	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	24.300	-6.500	90	Resistor	0Ohm
R24	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	25.400	-6.500	90	Resistor	10MOhm
R25	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	19.300	-9.400	270	Resistor	0Ohm
R26	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	18.300	-6.700	90	Resistor	10MOhm
R27	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	18.300	-9.400	270	Resistor	0Ohm
R28	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	20.300	-9.400	270	Resistor	10MOhm
R29	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	22.200	-9.300	90	Resistor	10MOhm
R30	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	23.300	-9.300	90	Resistor	0Ohm
R31	RC1005J000CS	RC1005J000CS	R1005-2PCB	TOP	26.500	-6.500	90	Resistor	0Ohm
R32	RC1005J103CS	RC1005J103CS	R1005-2PCB	TOP	27.600	-6.500	90	Resistor	10MOhm
R33	RC1005J103CS	RC1005J103CS	R1005-2PCB	BOTTOM	13.780	-6.110	180	Resistor	10MOhm
R34	RC1005J103CS	RC1005J103CS	R1005-2PCB	BOTTOM	11.570	-5.395	0	Resistor	10MOhm
R35	RC1005J103CS	RC1005J103CS	R1005-2PCB	BOTTOM	16.153	-7.410	180	Resistor	10MOhm
R36	RC1005J515CS	RC1005J515CS	R1005-2PCB	TOP	1.500	-18.310	180	Resistor	5.1TOhm

7. **Material Library**

Material Library menu lists materials library which could be used in PCB manufacturing. PollEx PCB supports default library list, but user can add new material or edit them. This material's properties can be used in **Signal Integrity** or **PCB Thermal** analysis. Use the menu, **Properties > Material Library**.

Materials

Name	Type	Frequency (MHz)	Dielectric Constant	Loss Tangent	Electric Resistivity (Ohm.m)	Relative Magnetic Permeability	Thermal Conductivity X (W/m.K)	Thermal Conductivity Y (W/m.K)	Thermal Conductivity Z (W/m.K)
AIR	Dielectric	0	1	0			0.0265	0.0265	0.0265
ALLOY42	Conductor	0			6e-07	1	12.5	12.5	12.5
ALUMINA94%	Dielectric	0	9	0.005			18	18	18
ALUMINA96%	Dielectric	0	9	0.005			35	35	29.4
ALUMINIUM-0TMPR	Conductor	0			2.73e-08	1	216.3	216.3	221.8
ALUMINIUM-6061T6	Conductor	0			2.73e-08	1	155	155	167
ALUMINIUM-NITRIDE	Dielectric	0	8.3	0.005			170	170	170
BERYLLIA	Dielectric	0	6.8	0.001			155.71	155.71	155.71
COPPER	Conductor	0			1.678e-08	1	370	370	394
FR4	Dielectric	0	4.5	0.02			0.35	0.35	0.35
GLASS-EPOXY	Dielectric	0	4.3	0.005			0.26	0.26	0.26
GOLD	Conductor	0			2.25e-08	1	297.2	297.2	297.2
INVAR	Conductor	0			8.33e-08	1	81.8	81.8	81.8
KOVAR	Conductor	0			4.9e-07	1	14.2	14.2	14.2
LEAD	Conductor	0			2.174e-08	1	32.7	32.7	32.7
MOLYBDENUM	Conductor	0			5.52e-08	1	142.3	142.3	142.3
MULLITE	Dielectric	0	6.4	0.005			6	6	6
NICKEL	Conductor	0			7.16e-08	1	92	92	92
PLATINUM	Conductor	0			1e-07	1	71.6	71.6	71.6
POLYIMIDE	Dielectric	0	4.5	0.01			0.26	0.26	0.26
SILICON	Conductor	0			3160	1	83.7	83.7	83.7

Import Export Remove Add Dielectric Add Conductor Edit OK Cancel

Default library file's location is
`C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Data\Default_material.mtrl`.

8. **Layer Stack**

Layer Stack menu shows PCB's physical stack up structure. User can edit each layer's type, material and thickness. User can also import, export, add, remove and insert. This information will be used in **PollEx SI** and **PollEx Thermal** analysis. Use the menu, **Properties > Layer Stack**.

Layer Stack

Layer Stack

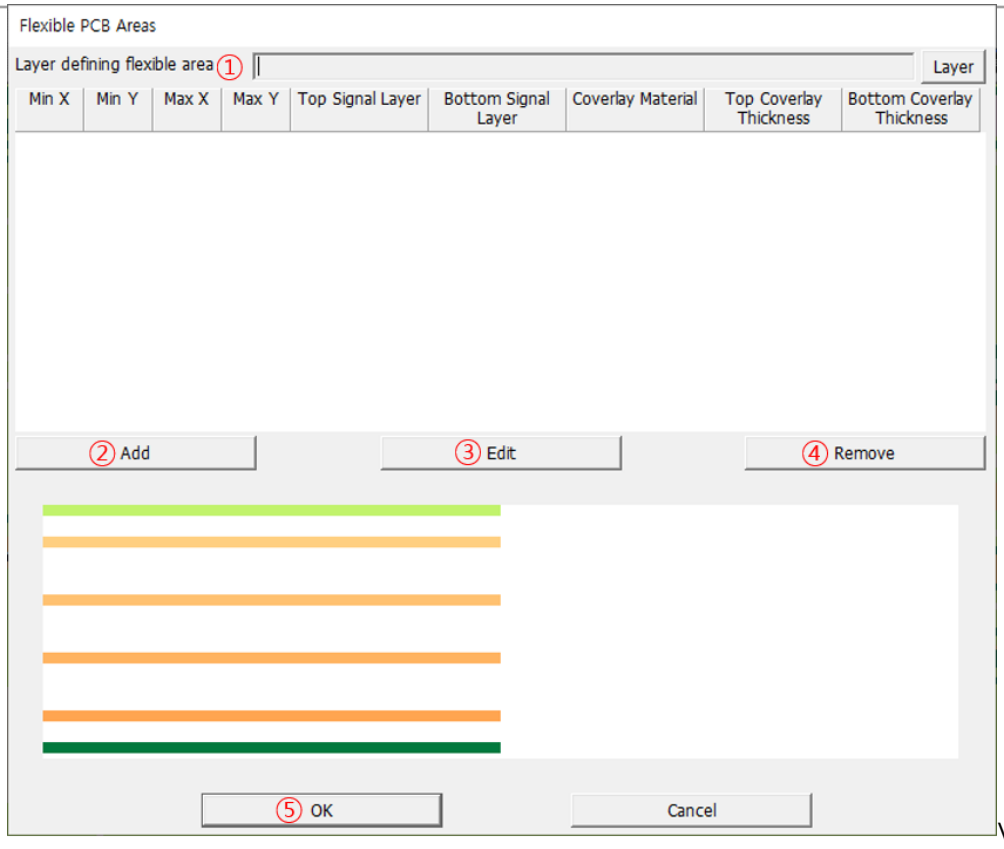
No.	Name	Type	Thickness (mm)	Conductor Material	Dielectric Material	Color	Trace Width Etching Difference (mm)	Wider Trace Side
1	1	Ground	0.035	COPPER	AIR		0	BOTTOM
	Dielectric Layer	Dielectric	0.065		FR4		0	BOTTOM
2	2	Ground	0.035	COPPER	FR4		0	BOTTOM
	Dielectric Layer	Dielectric	0.15		FR4		0	BOTTOM
3	3	Ground	0.035	COPPER	FR4		0	BOTTOM
	Dielectric Layer	Dielectric	0.15		FR4		0	BOTTOM
4	4	Ground	0.035	COPPER	FR4		0	BOTTOM
	Dielectric Layer	Dielectric	0.15		FR4		0	BOTTOM
5	5	Power	0.035	COPPER	FR4		0	BOTTOM
	Dielectric Layer	Dielectric	0.065		FR4		0	BOTTOM
6	6	Ground	0.035	COPPER	AIR		0	BOTTOM

Total thickness (mm) 0.79

Import Export Add Remove Insert Export MS Excel Apply OK Cancel

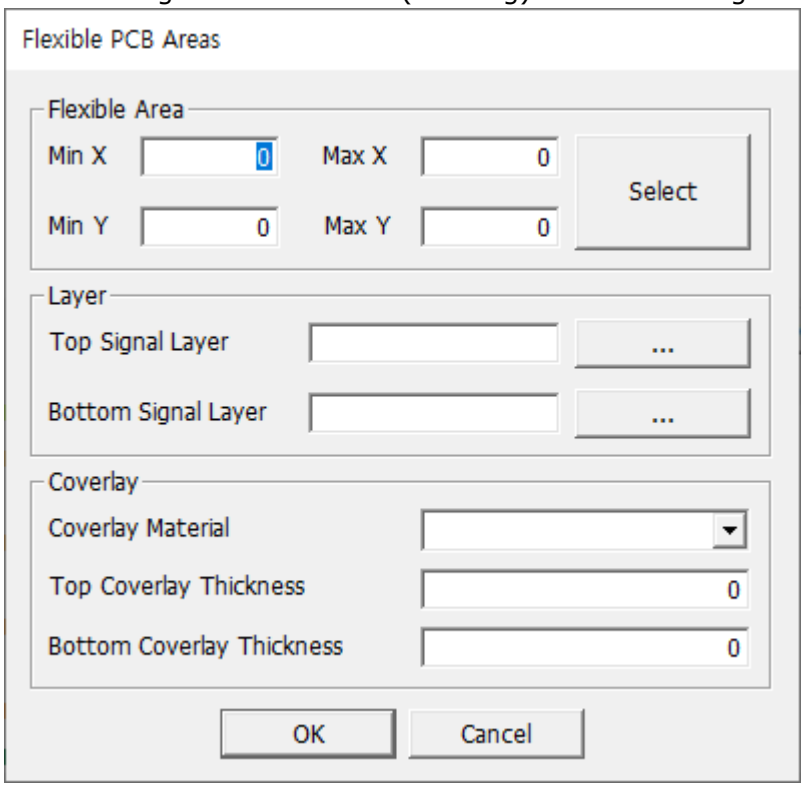
9. Rigid-Flexible PCB

Define the flexible area of the rigid-flexible PCB.



① Layer defining flexible area: Designate the artwork layer (NOT physical layer) that is set as the flexible area
Find the objects in the layer and automatically record them in the table.

② Add: Settings for the flexible (bending) area on the Rigid-flexible PCB design



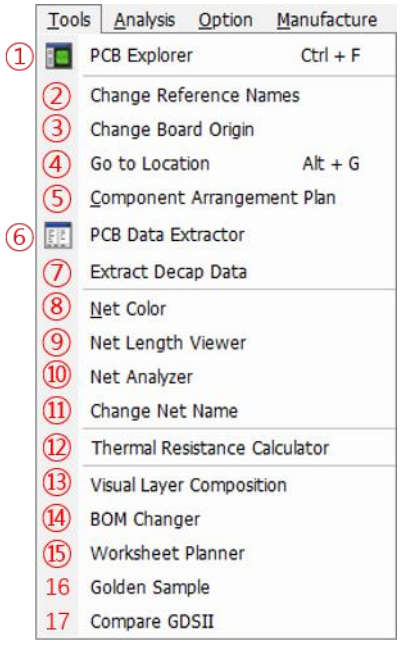
- Flexible PCB Area: Set the layer where the bending area is designed, or the user sets the area.

- Layer: The flexible layer is defined as the starting and ending layers of the physical layer.
- Coverlay: Set the Coverlay property information.

③ Edit: Modify the saved settings.
④ Remove: Delete the saved settings from the lists.
⑤ Press the OK button to save the settings.

Tools

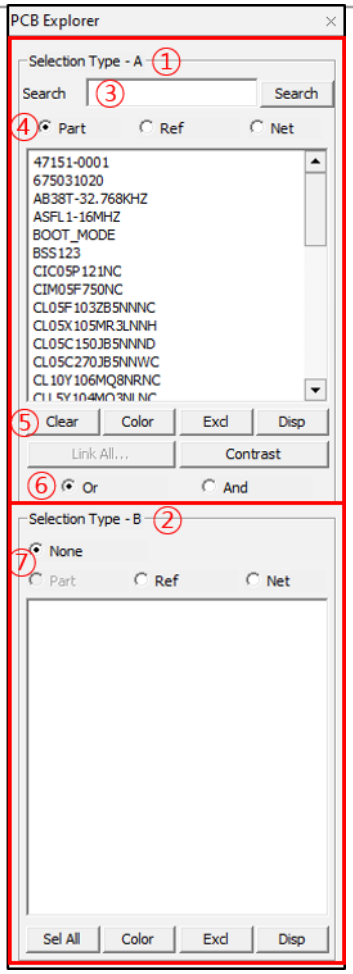
Under **Tools** menu, there are many useful functions. Almost functions help users to get documents or reports for nets or components.



① PCB Explorer
② Change Reference Names
③ Change Board Origin
④ Go to Location
⑤ Component Arrangement Plan
⑥ PCB Data Extractor
⑦ Extract Decap Data
⑧ Net Color
⑨ Net Length View
⑩ Net Analyzer
⑪ Change Net Name
⑫ Thermal Resistance Calculator
⑬ Gerber Transformation
⑭ Visual Layer Composition
⑮ BOM Changer
16 Worksheet Planner
17 Golden Sample
18 Compare GDSII

1. PCB Explorer

PCB Explorer helps user to search components or nets. Also, it provides searching objects of combination for net and net connected components or component and connected nets. Use the menu, **Tools > PCB Explorer**.



① **Selection Type – A**: Basic search window (Type-A).
② **Selection Type – B**: Second search window (Type-B).
③ Searching keyword input box. If user wants to search the **Part**, **Reference** or **Net** name, use this. Also, users can search keyword input box with Wild Card(*, ?, #) in PCB Explorer. Search keyword is case-insensitive.
***:** String
?: One Character
#: One Number
" ": Searching the matching string only.
④ Objects selection in the basic search window.
Example 1) Search String: c1
Search Result: *C1, C10, C11, IC1, IC10, IC11 etc.

Example 2) Search String: gr red blu
Search Result: GREEN, GREEN1, RED, RED1, BLUE, BLUE1 etc.

Example 3) Search String: "green" "red" "blue"
Search Result: GREEN, RED, BLUE

Example 4) Search String: 1*
Search Result: 1S335-BP, 1SV164 etc.

Example 5) Search String: *1*
Search Result: 1S335-BP, 1SV164, AD724JR-16-IC, ERJ6GEYJ101, ERJ6GEYJ301, ERJ6GEYJ331 etc.

Example 6) Search String: ?#1#
Search Result: C210, C211, C212, R214, U210 etc.

Example 7) Search String: ?c5
Search Result: *C5, IC5 etc.

Example 8) Search String: "c6""
Search Result: C6"

Including Wild Card(*, ?, #) in string, enter " ' " ahead of the Wild Card.
Not including Wild Card(*, ?, #) in string, " ' " is regarded as the character.

Example 1) Search String: CLK'*
Search Result: CLK*

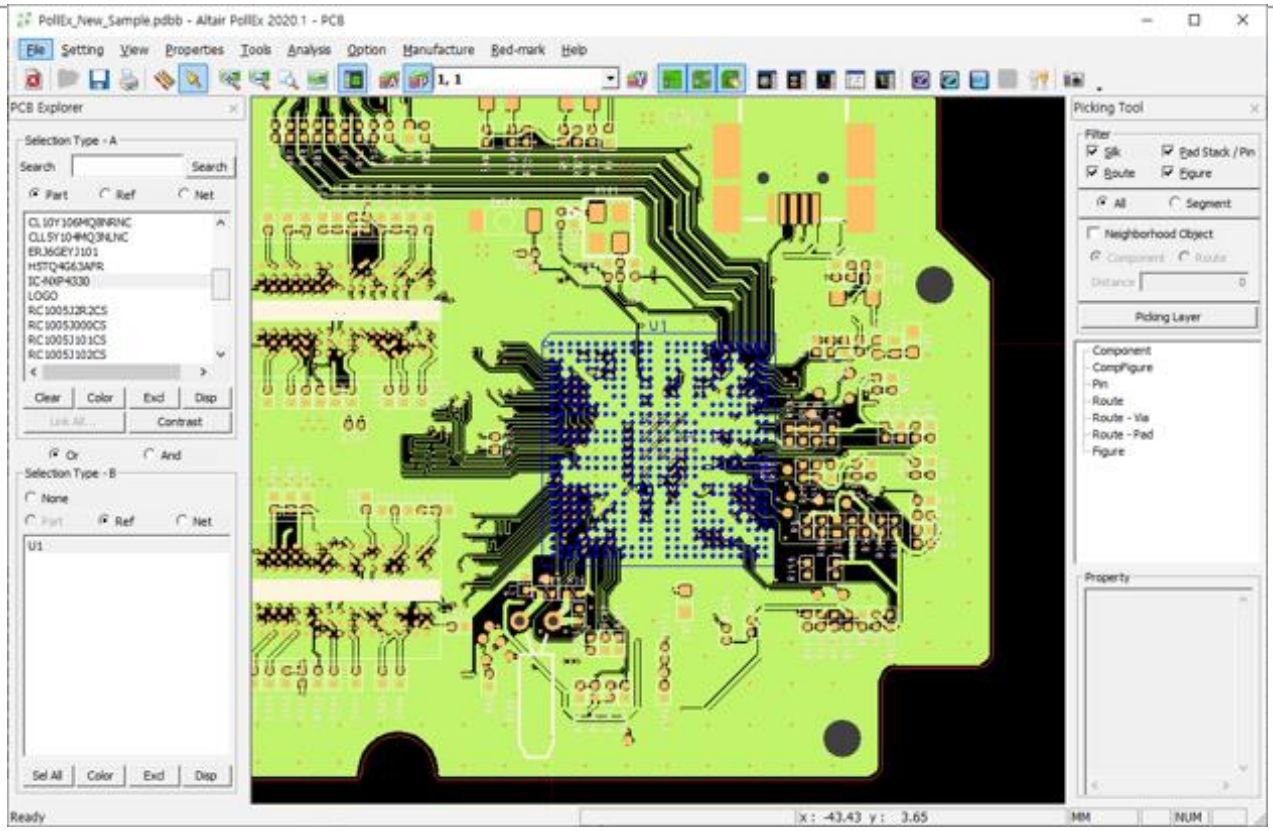
Example 2) Search String: CLK'A
Search Result: CLK'A

⑤ View control buttons on screen.
Clear: reset selection.
Color: assign color for selected objects.
Excl: display only selected objects. For others, PollEx PCB will not show them.
Disp: make high-light for selected objects.
Contrast: display unselected objects with gray color.

⑥ Combination methods selection for objects on basic window and second window.

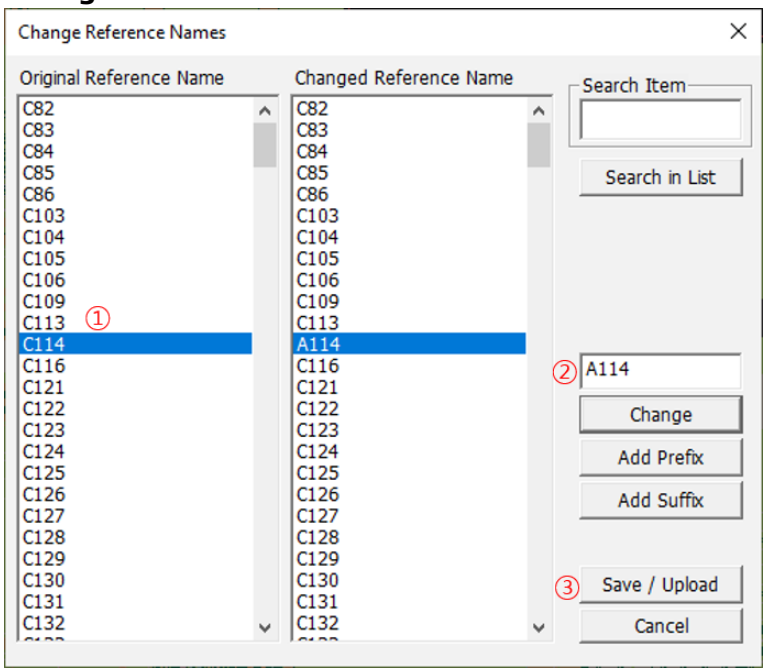
⑦ Second window's object selection.

Basically, PollEx PCB Explorer runs with two windows, ① and ②. If user wants to search certain objects on PCB, using **Selection Type-A** would be enough. However, if user wants to find a certain net and connected components for selected net, use **Selection Type-B**. In this case, select with **Net** in the **Selection Type – A** and Ref in the **Selection Type – B**.



2. **Change Reference Names**

If user wants to change the reference name, use this function. But, once reference name is changed, inner data structure is also changed. So be cautious to use this function. Use the menu, **Tools > Change Reference Names**.



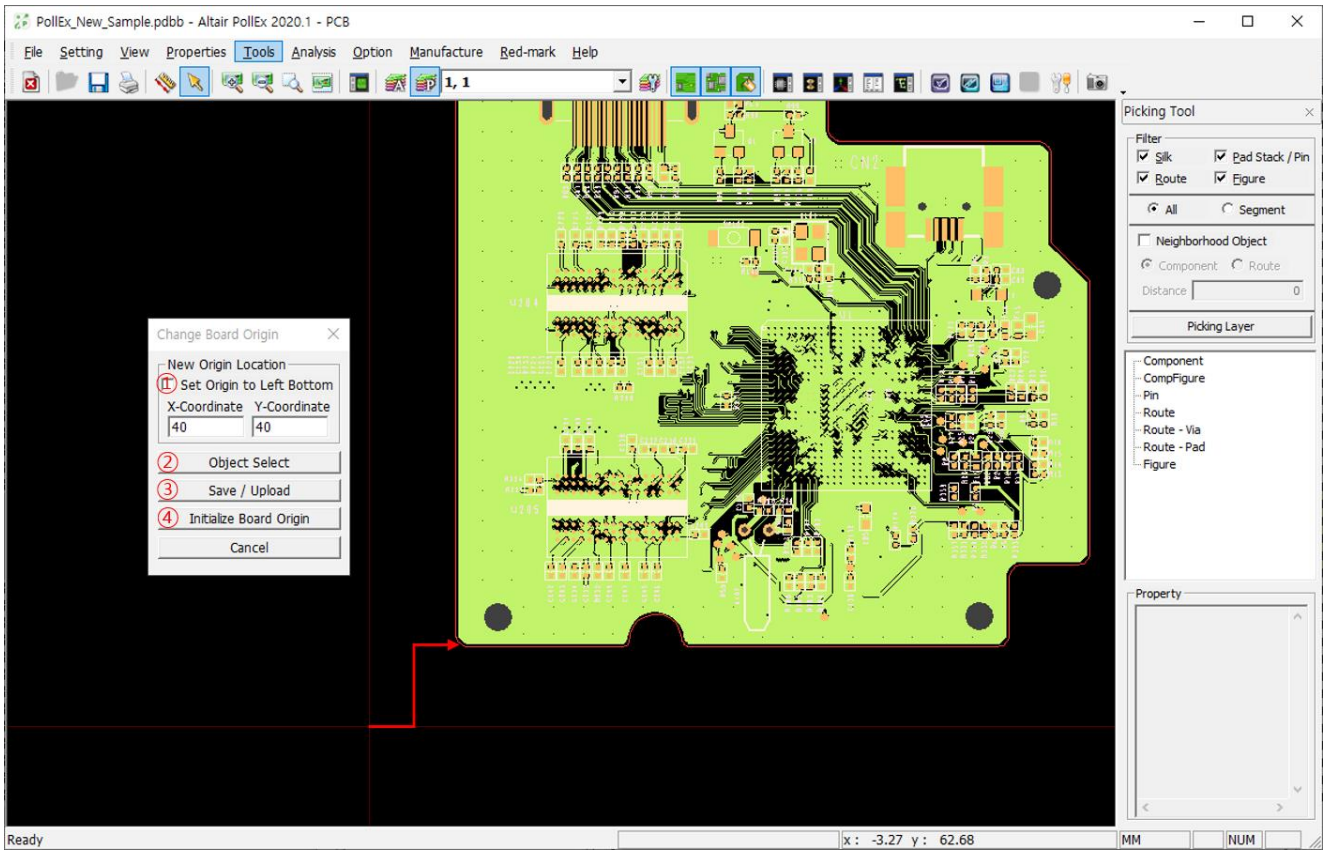
① Select reference which user wants to change reference name.

② Give target string to be changed and press action button among **Change**, **Add Prefix** or **Add Suffix**.

③ Press **Save/Upload** button change and save for update.

3. **Change Board Origin**

If the origin point of PCB design is incorrect, user can change its origin point with this function. Use the menu **Tools > Change Board Origin**.



① Origin and left bottom of board outline are away. If checking **Set Origin to Let Bottom** button, move origin based on left bottom of board outline. At this time, difference is calculated, it can see values in X, Y-Coordinate.

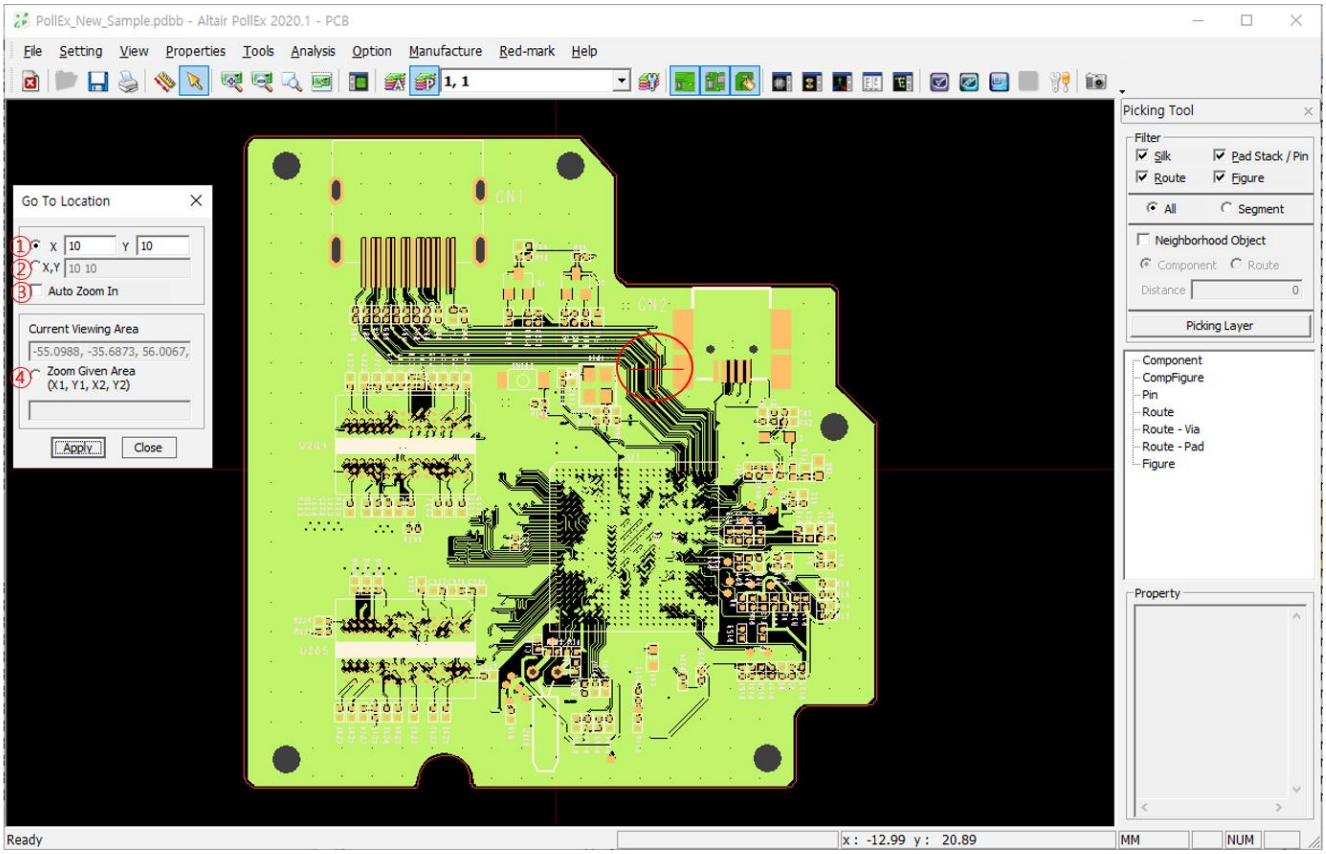
② Object Select: Select the object to be origin.

③ After specifying new origin point, pressing **Save/Upload** button will change the origin point of board.

④ To go back to initial status, use the button, **Initialize Board Origin**.

4. **Go to Location**

If user moves mouse cursor to certain point, use this function. Use the menu, **Tools > Go to Location** (Shortcut key: **Alt + G**).



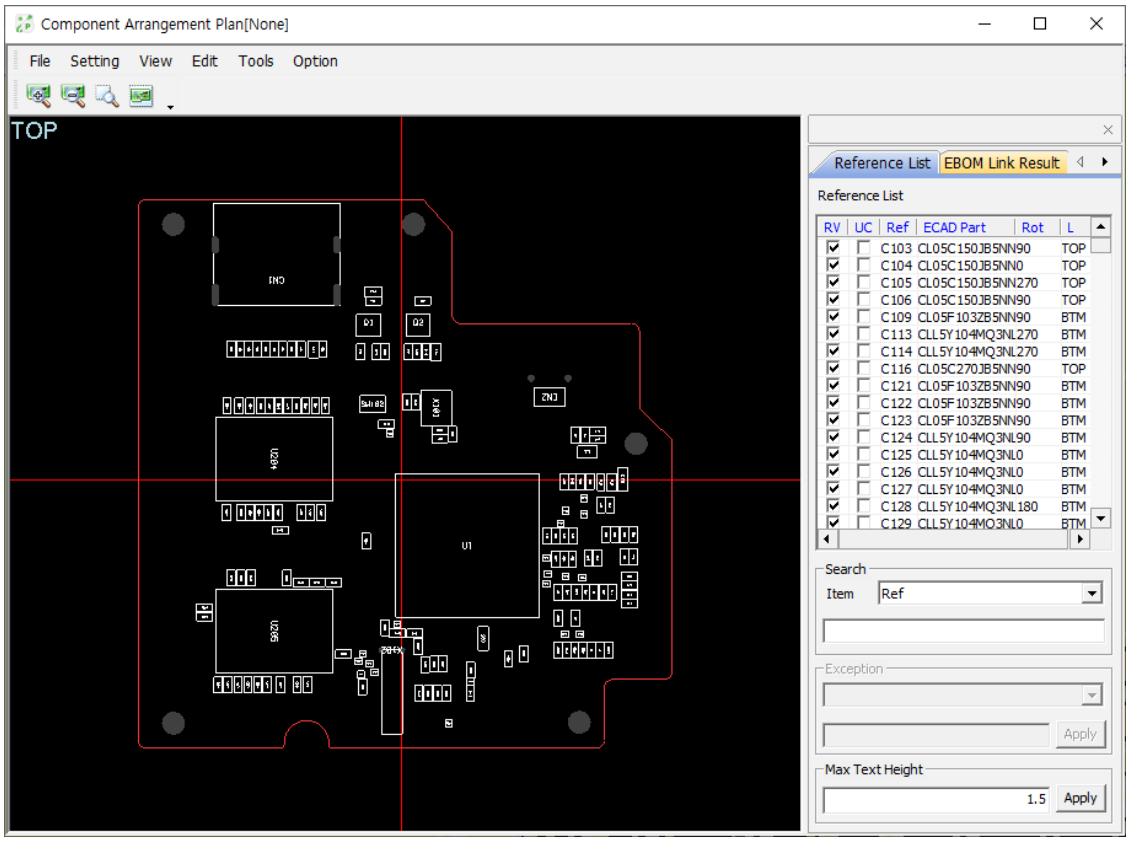
① Give the target location to which user wants to move mouse cursor.
② Also, at this column, user can give location from paste function from other application.
③ If checking **Auto Zoom In**, give the target location with auto zoom-in.
④ Setting two locations will zoom in screen with rectangle area with given two points.
⑤ **Apply** button will do action.

To input location with manually, x and y locations should be separated with "**,**"(comma). After **Apply** action, searched location will remain with "+" mark until the window is closed.

5. **Component Arrangement Plan**

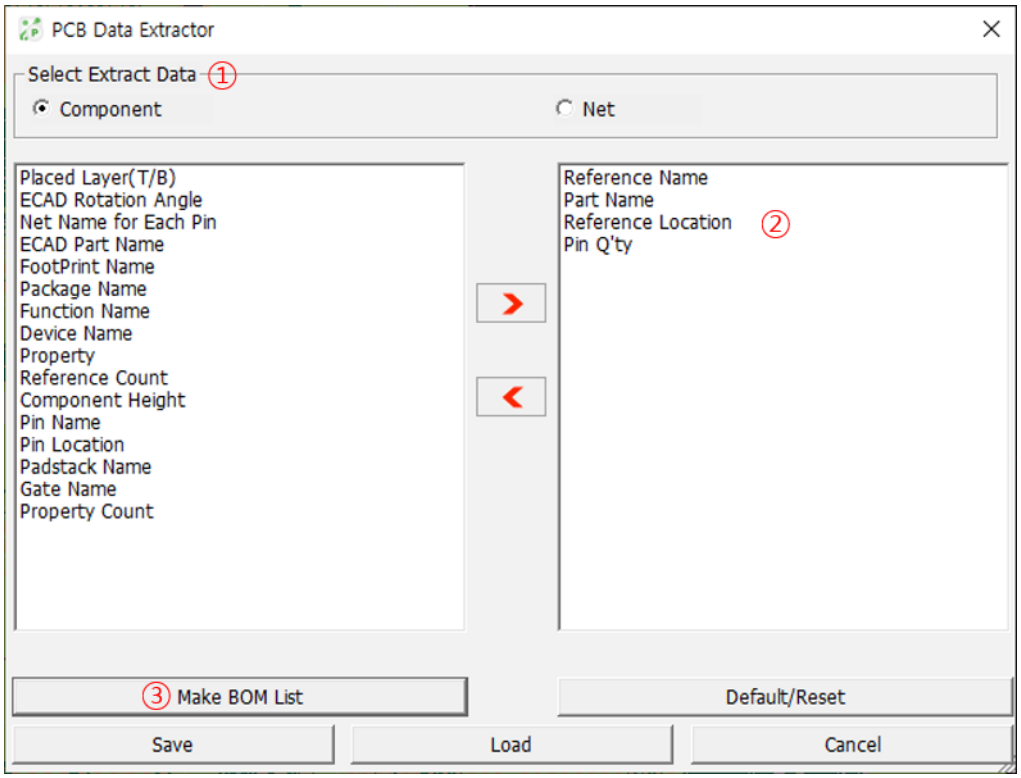
This function gives user to replace paper type worksheet into report. This function shows on-board components with their area and marking at 1st pin. In addition, there are other useful functions. Use the menu, **Tools > Component Arrangement Plan**.

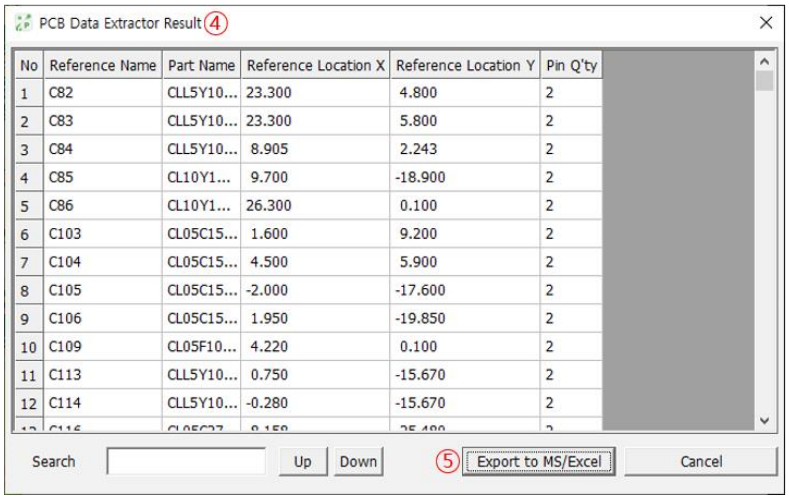
Refer to the **Component Arrangement Plan** manual for detail instructions.

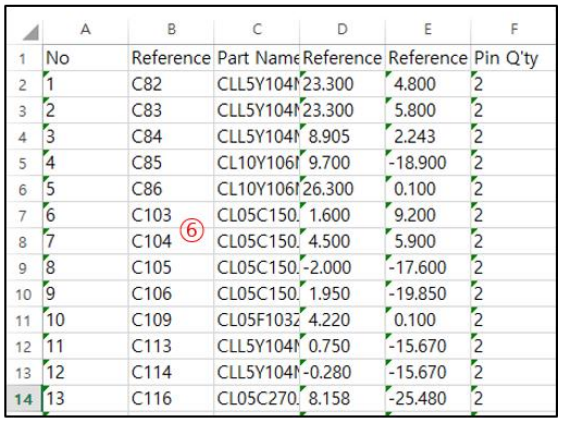


6. **PCB Data Extractor**

As a powerful documentation function, using this function, user can export PCB information into MS/Excel file. Target information may be nets, components and their relating properties. Use the menu, **Tools > PCB Data Extractor**.



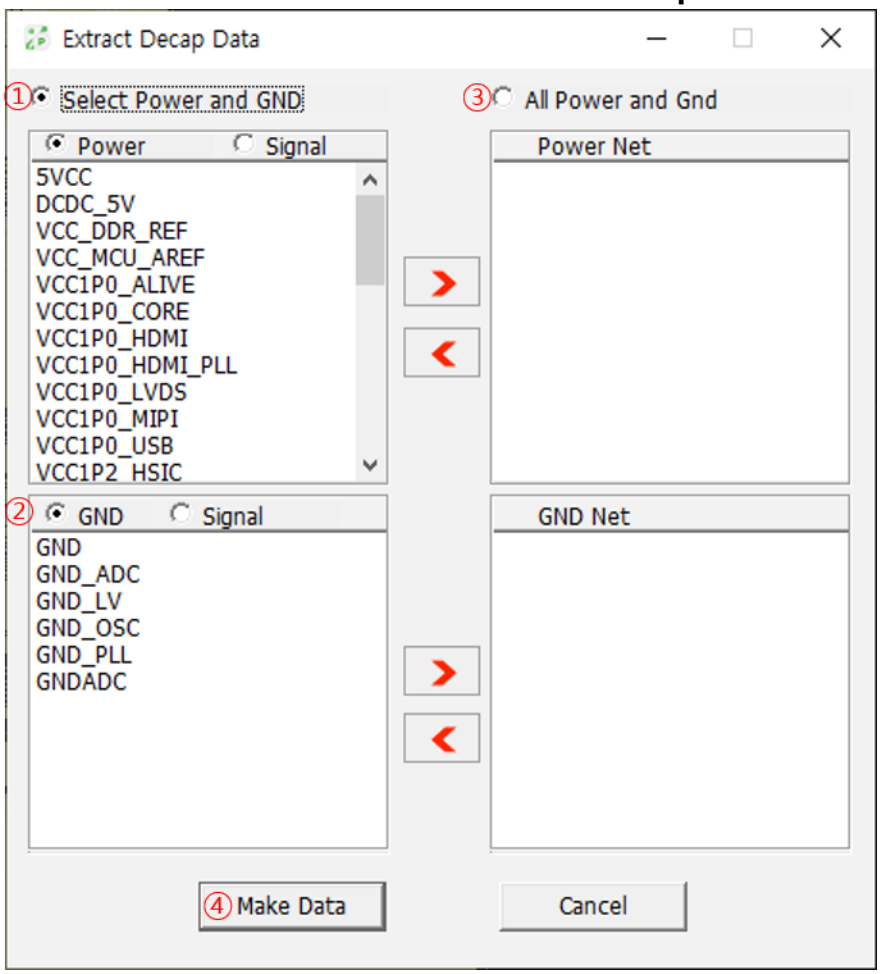




① At the dialog window, **PCB Data Extractor**, select extraction type between **Net** and
② **Component**.
③ If user selects extraction type, dialog window show properties list at left list-control box. Select properties to be extracted as order to match.
④ Pressing button menu, **Make BOM List**, shows table-driven document form.
⑤ User can check the output form.
⑥ Pressing button menu, **Export to MS/Excel** makes MS/Excel sheet.
⑦ Check result document.

7. **Extract Decap Data**

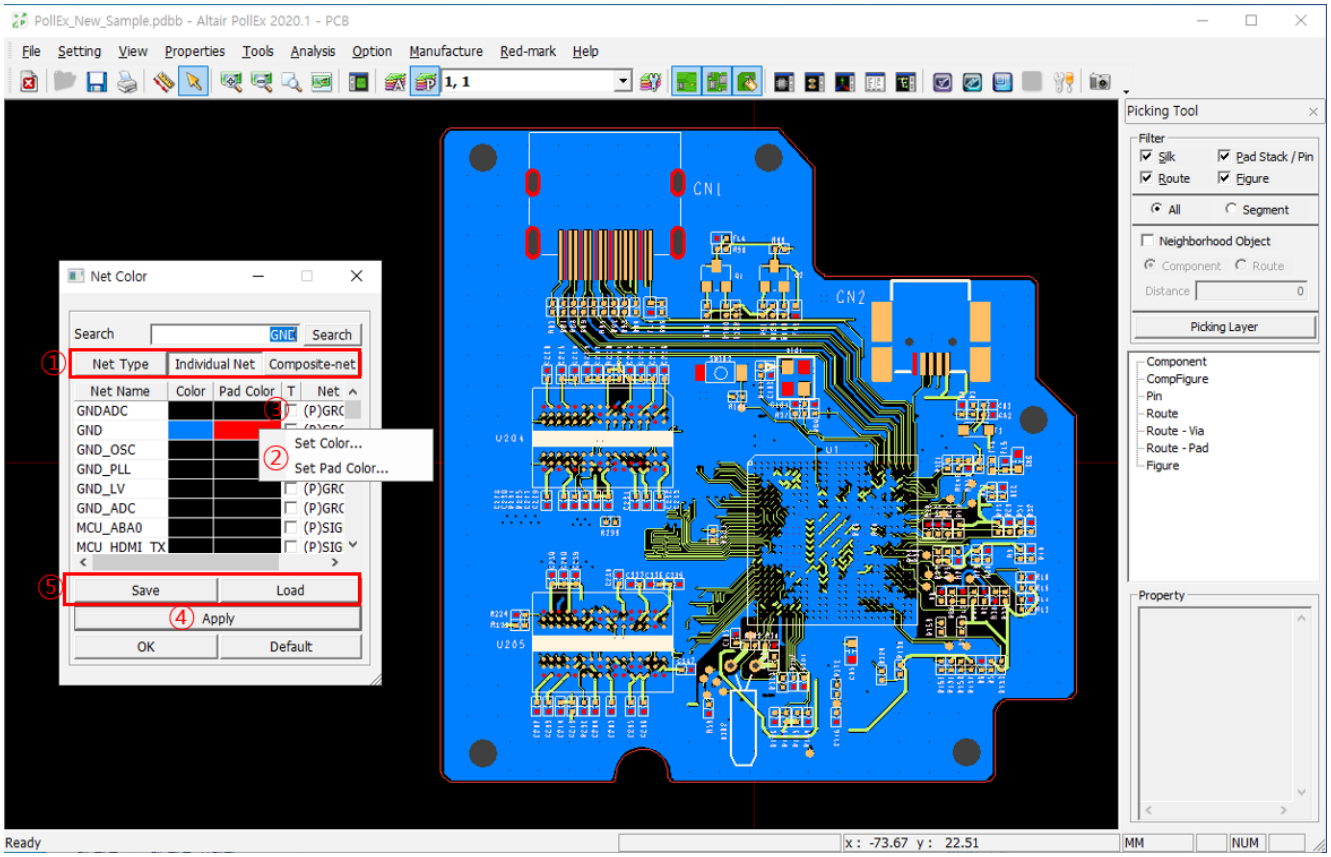
Decoupling capacitor (By-pass capacitor) is capacitor device which connect power and ground nets for the purpose of making stable power supplying. PollEx PCB has the feature to find them in PCB and make its result into document. Use the menu **Tools > Decap Extractor**.



① Select power nets among list.
② Select ground nets among list.
③ Selection for all power/ground nets in design.
④ Button menu, **Make Data** show list of de-coupling capacitors.

8. **Net Color**

Users can change the color of net(s) to make it easier for exploring PCB design. Use the menu, **Tools > Net Color**.



① Select net classification.
Net Type: Net sorting depending on net type. Ex) power/ground/signal
Individual Net: Net sorting depending on net name.
Composite-net: Net sorting for composite-nets.

② After selecting net(s), use the mouse right button. And at pop-up menu, use **Set Color** to select certain color.

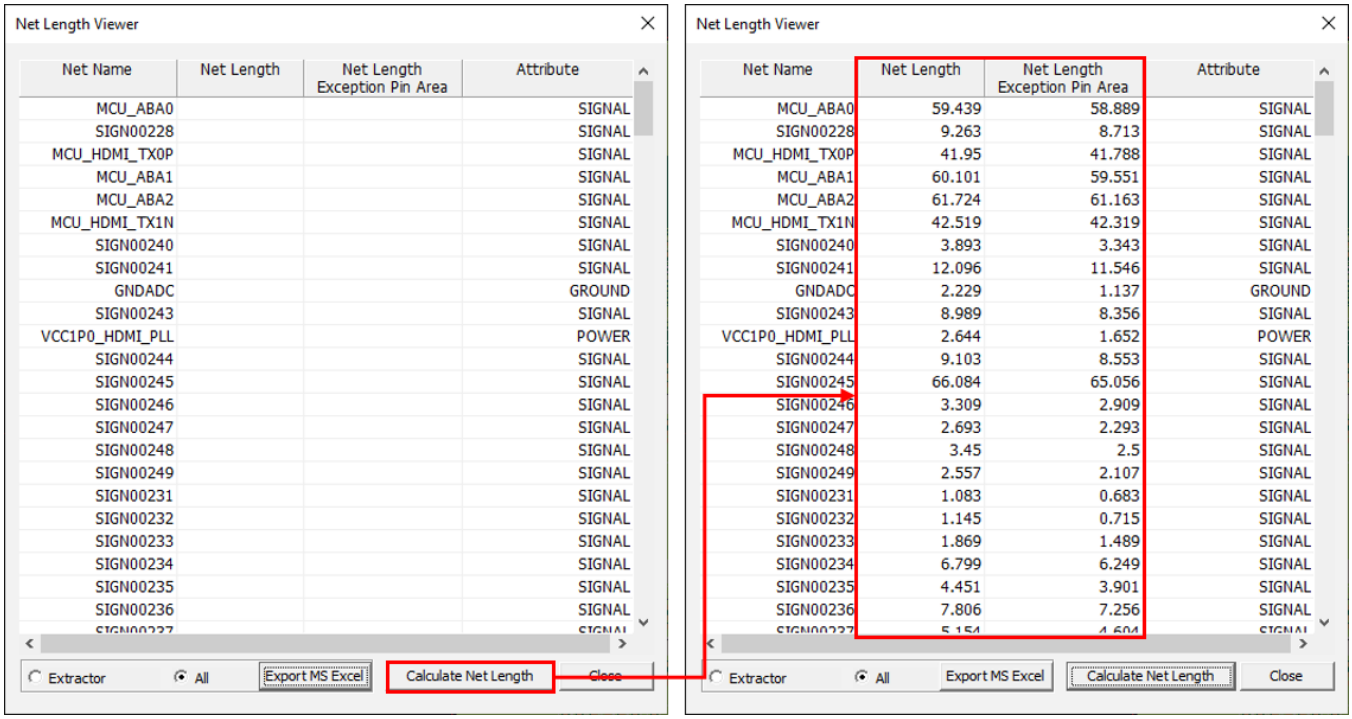
③ If checking "**T**", make transparent selected net status.

④ Pressing button menu, **Apply** will apply changing into design.

⑤ Save the setting of defined color to file(*NCLR). And to use this change at next design opening, check the **Load** and **OK** button.

9. Net Length Viewer

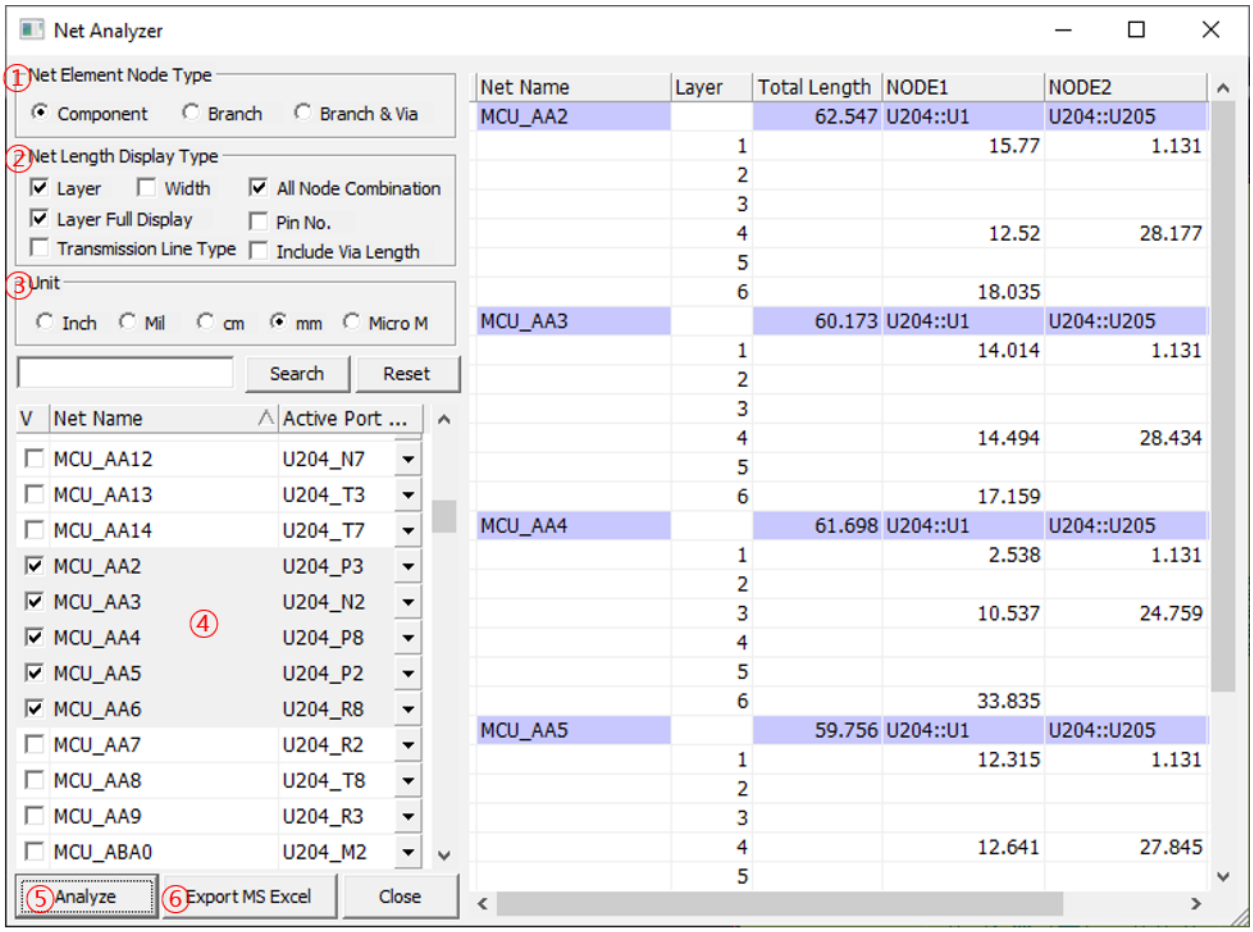
PollEx PCB extracts report for all nets' length on design. Use the menu, **Tools > Net Length View**.



※ The meaning of **Net Length** is summation of routing pattern's segments. But it does not include the copper pour size. Use the button menu, **Export to Excel** to make list into MS/Excel sheet.

10. Net Analyzer

PollEx PCB makes report for net length analyzing feature. For total net length, user can extract report for segment length on certain layers, to the branching points and to the via(s). Use the menu, **Tools > Net Analyzer**.



① Select element type to make nodes.
Comp: Net length among components.
Branch: Net length among components and branching points.
Branch & Via: Net length among components, branching points and vias.

② **Net Length Display Type**: Select desirable objects in report.
Layer: Shows length depending on layer.
Width: Shows routing pattern's width.
All Node Combination: Shows all combinations of nodes.
Layer Full Display: Shows stack-up information and each layer's length.
Pin No: Shows components' pin number also.
Transmission Line Type: Shows transmission line type, not Layer.
Include Via Length: Shows including via length.

③ Select unit.

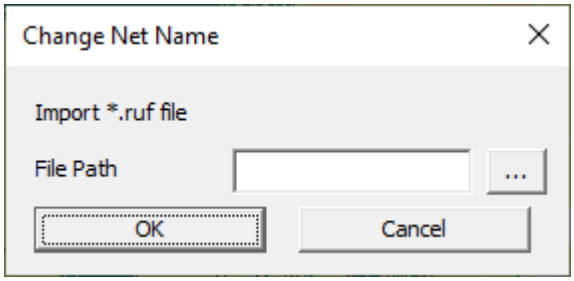
④ Select target net(s).

⑤ Press **Analyze** button will make analyzing report for selected target net(s).

⑥ Press **Export to Excel** button will make report to MS/Excel sheet.

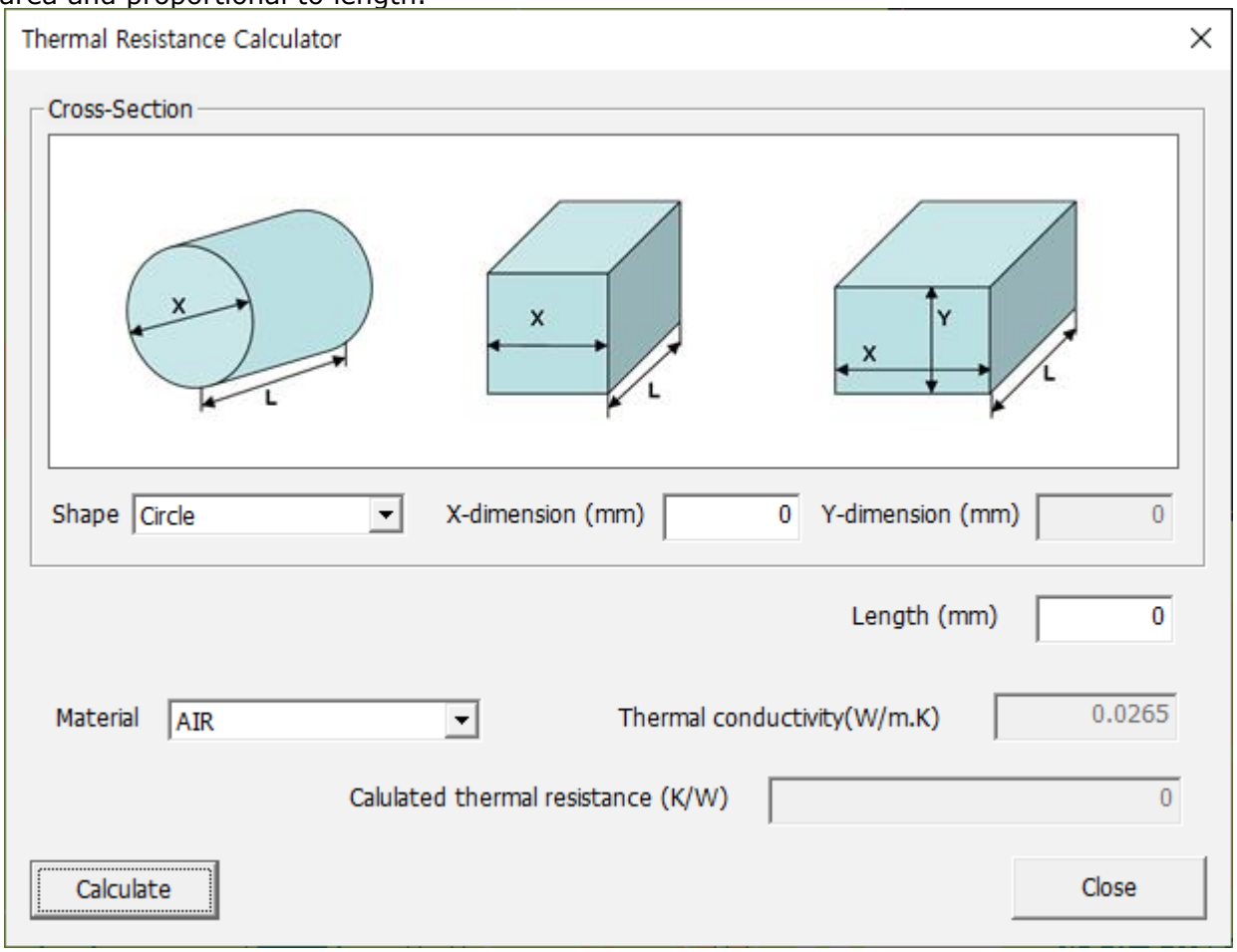
11. **Change Net Name**

In case of Zuken Board Designer Interface, it is possible to change the net name of PCB layout from `*.ruf` file. It can be changed on PDBB. Only same pin connection will be changed. Use the menu, **Tools > Change Net Name**.



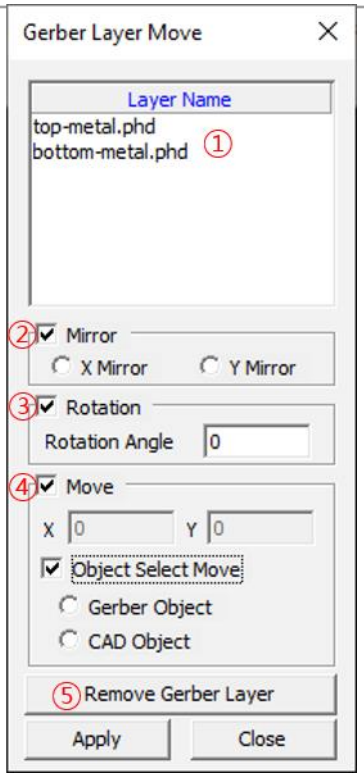
12. Thermal Resistance Calculator

Can calculate thermal resistance value of given material by "Thermal conductivity".
Select the shape of target material among circle, square, rectangle, and then give each value for X-dimension (mm) and Y-dimension (mm), Length (mm). Thermal resistance is inversely proportional to area and proportional to length.



13. Gerber Transformation

After importing Gerber data, and then user can move or mirror the location of it. To use this menu, go to **Tools > Gerber Transformation.**



① **Layer Name:** Lists up the Gerber layers. Select the target layer on here.

② **Mirror:** Shows the mirrored Gerber data.

③ **Rotation:** Shows the rotated Gerber data.

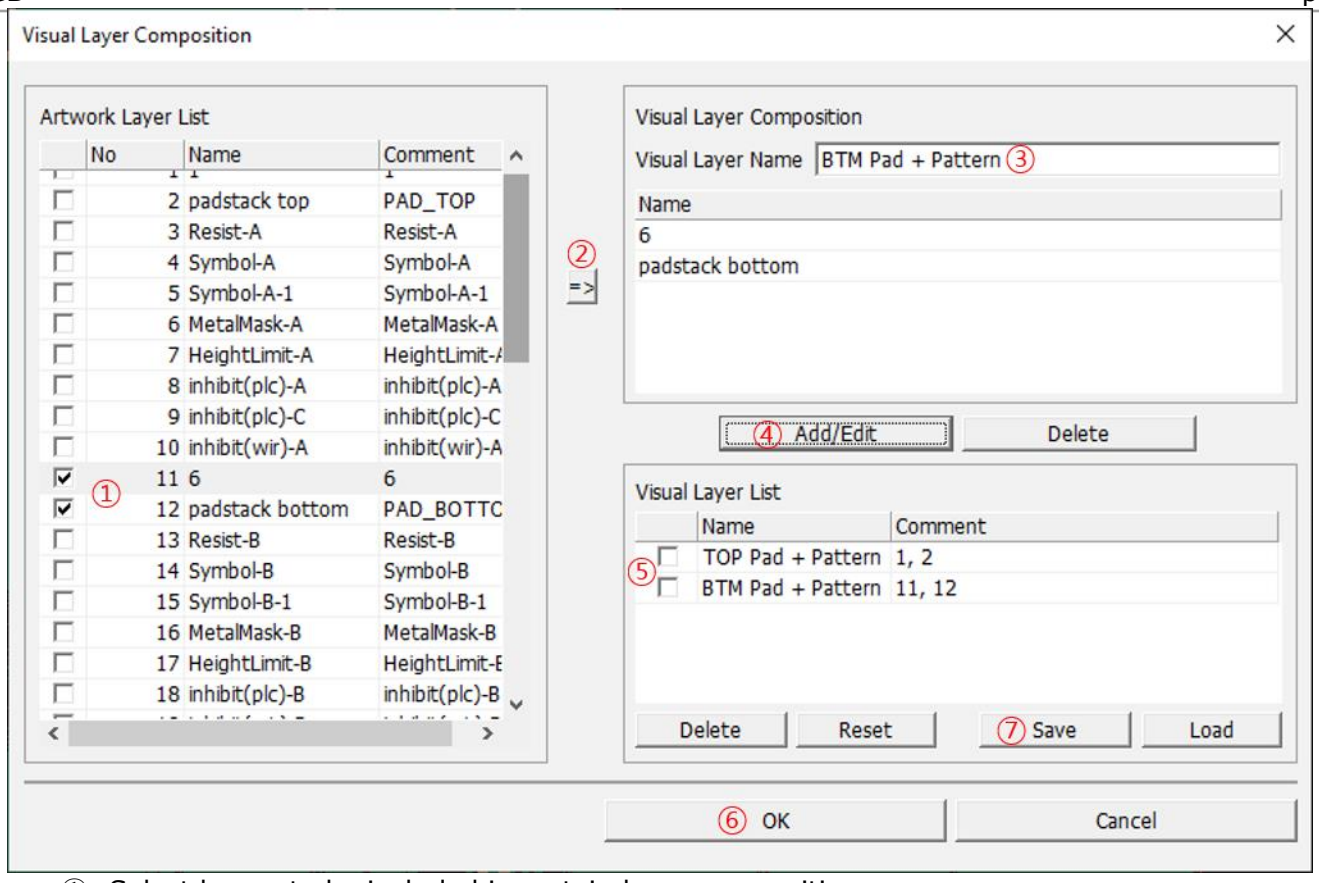
④ **Move:** Enter the X and Y coordinates to move the Gerber data.
Object Select Move: Calculates the coordinate difference between Gerber and PCB data.
Gerber Object: Select Gerber Object on the screen, and select the object of the PCB data (the location is to move the Gerber data.).
CAD Object: Select the PCB object on the screen and select the object of Gerber data (the location is to move the PCB data).

⑤ **Remove Gerber Layer:** Deletes the Gerber Layer.

⑥ **Apply:** The settings are reflected on the screen.

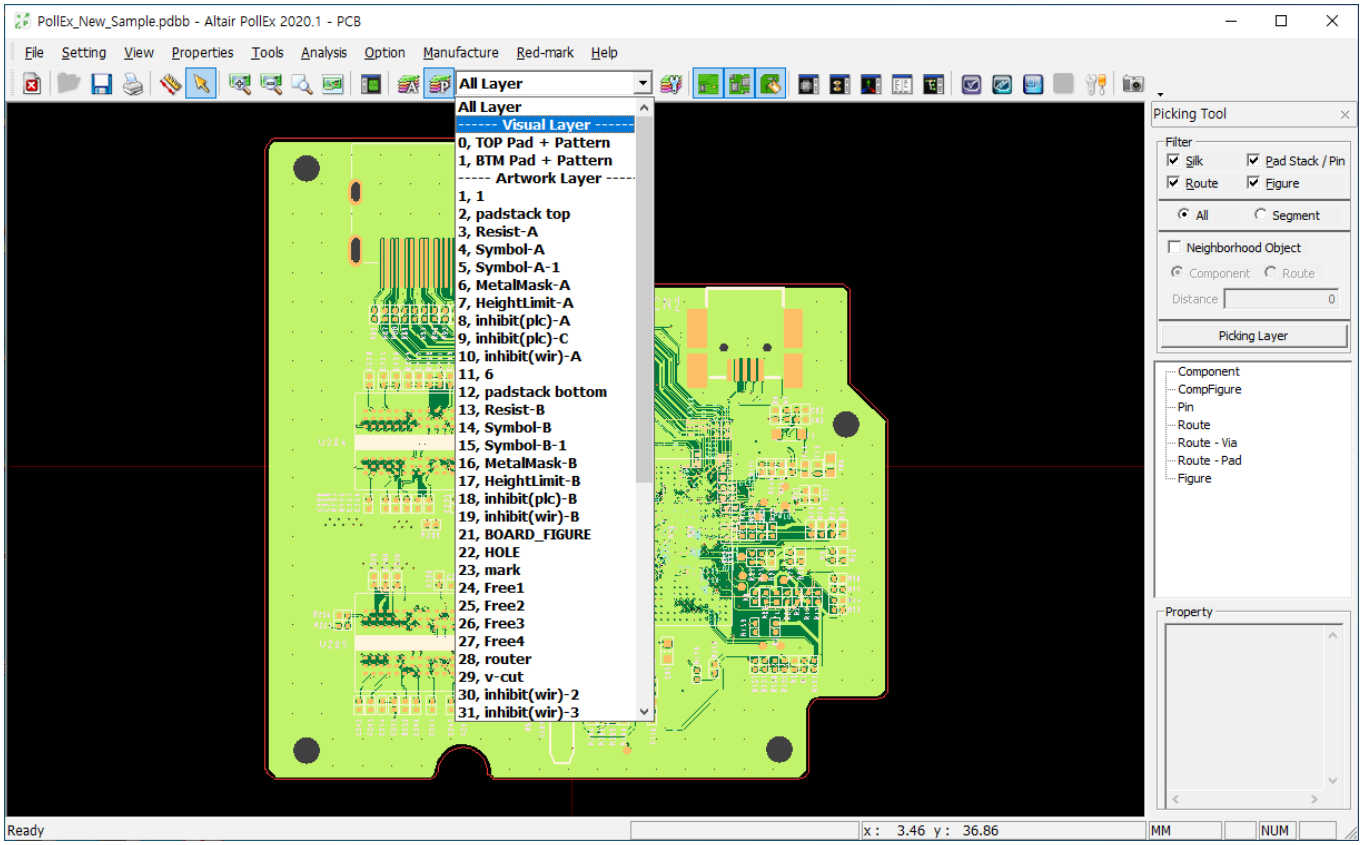
14. **Visual Layer Composition**

User can layer pairs to be displayed at same time. To make layer pairs(composition), use the menu, **Tools > Visual Layer Composition**.



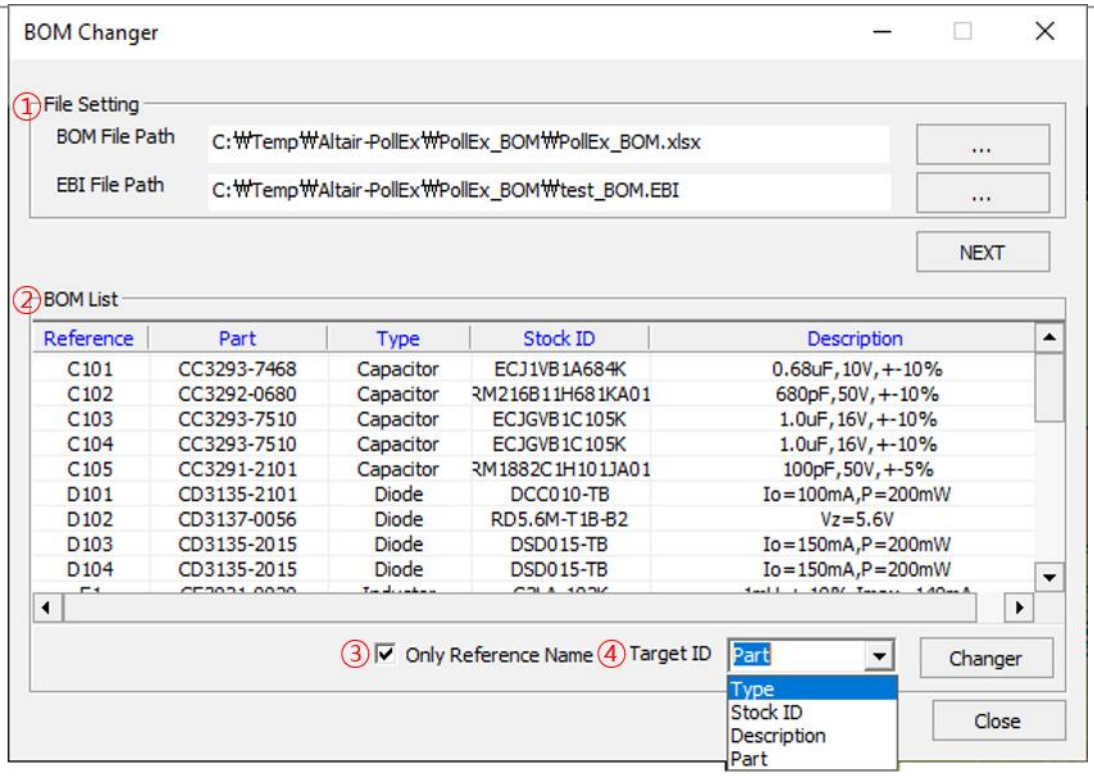
① Select layers to be included in certain layer composition.
② Pressing this button means selected item will be potential target nets. Selected layers will be copied to the list in **Visual Layer Composition** window.
③ Give the name of (layer) composition.
④ **Add/Edit** button will make new layer composition item. And, show it in **Visual Layer List** window.
⑤ At **Visual Layer List** contains current layer composition list.
⑥ **OK** button will complete task.
⑦ **Save** button will save current setting into the file, `*.vls`. In other design, PollEx PCB will load this setting for reviewing design.

※ Users can see this layer composition in Layer Set-up window with artwork layer order list. See the following picture.

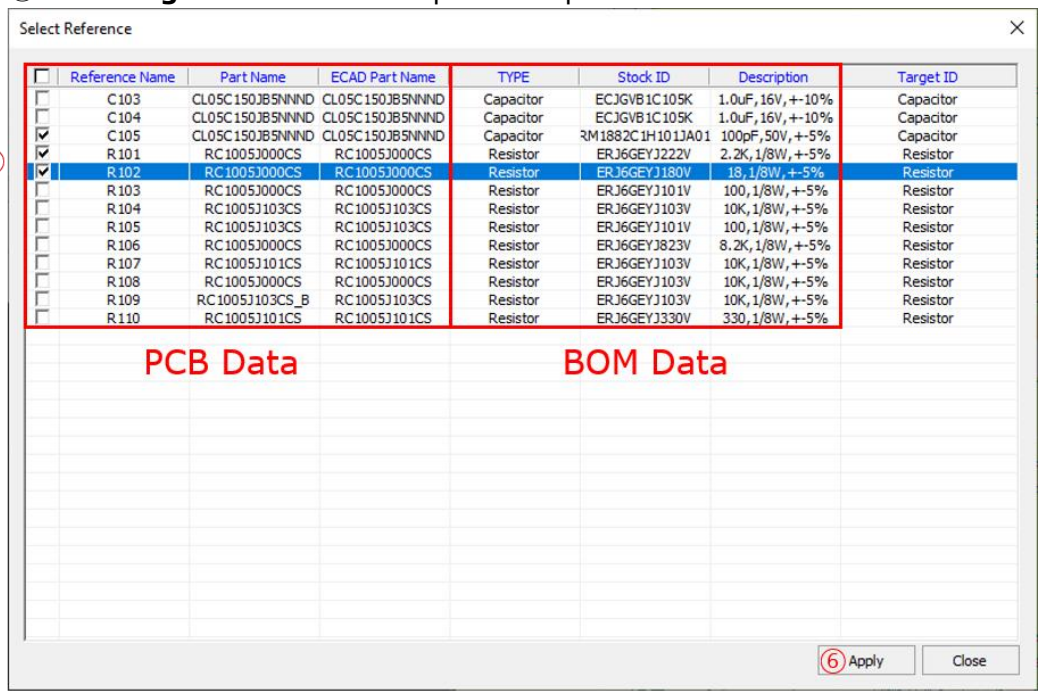


15. **BOM Changer**

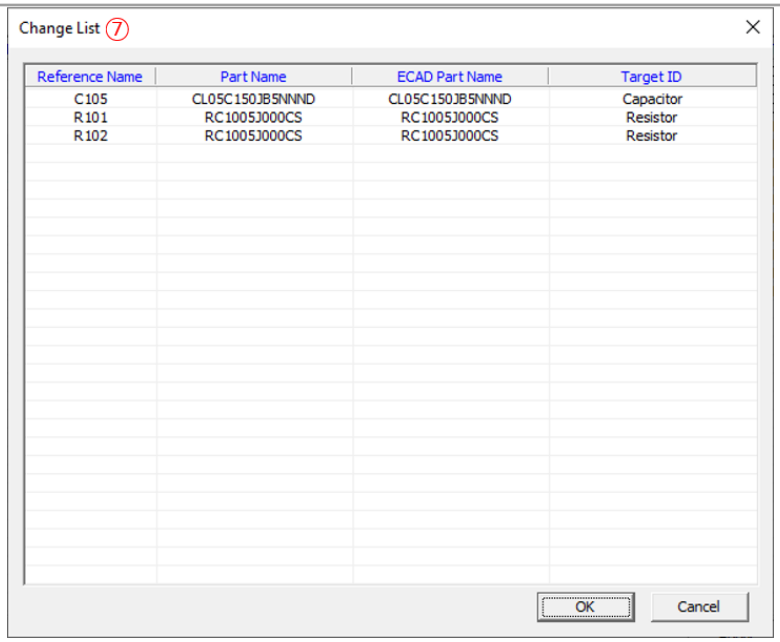
BOM Changer can be substituted for part name as part name in the BOM file. It can be modified to match each other by utilizing Reference Names between the PDB Data and BOM file. Use the menu, **Tools > BOM Changer**.



① Select BOM file(`*.xls`) and EBI file. And press **Next** button.
② The contents of BOM file is displayed.
③ In case of this option is checked, if the reference name is matched with PCB Data and BOM, it will be listed. In case of this option is un-checked, if the reference name and ECAD part name are matched with PCB Data and BOM, it will be listed.
④ Set **Target ID** of BOM to replace the part name of the PDB Data.



⑤ Check the list to change.
⑥ Press **Apply** button. Then the result will be pop-up.



⑦ Show the changed list. Replace the ECAD part name of the PDB as Target ID. And press "OK" button.

⑧ If pressing "OK" button, apply ECAD part name of PDB will be changed. If pressing "Cancel" button, return to the previous status.

16. Worksheet Planner
Use the menu, **Tools > Worksheet Planner**.
Refer to the **Worksheet Planner** manual for detail instructions.

17. Golden Sample
Use the menu, **Tools > Golden Sample**.
Refer to the **Golden Sample** manual for detail instructions.

18. Compare GDSII
Use the menu, **Tools > Compare GDSII**.
Refer to the **Compare GDSII** manual for detail instructions.

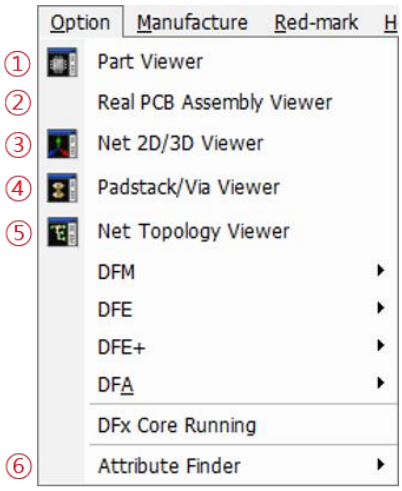
Analysis

1. **Signal Integrity**
2. **Power Integrity**
3. **Radiated Emission**
4. **Thermal**

For above features, refer to individual manual for those products.

Option

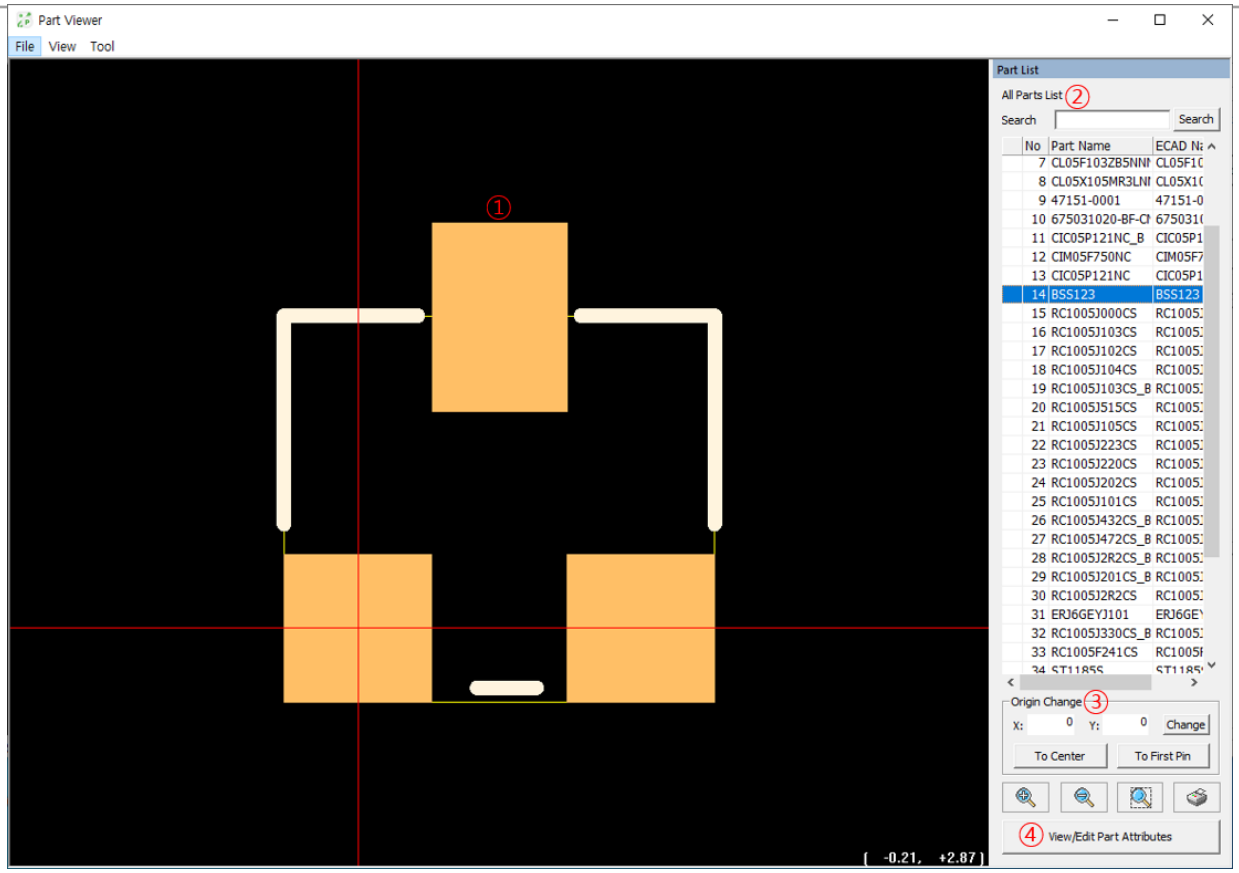
PollEx PCB supports different viewers for reviewing objects on board. And it has communication toolset with which engineers in remote location can share their idea with watching same screen.



① Part Viewer
② Real PCB Assembly Viewer
③ Net 2D/3D Viewer
④ Padstack/Via Viewer
⑤ Net Topology Viewer
⑥ Attribute Finder

1. **Part Viewer**

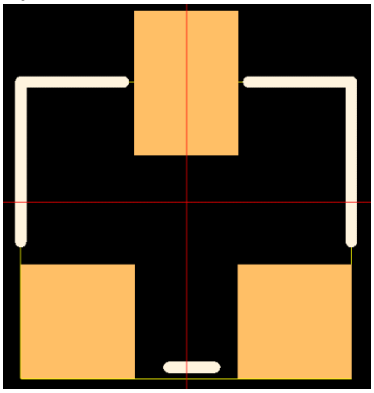
Part Viewer is viewer for part library used in current design. It also shows used padstack type and padstack size. Used the menu, **Option > Part Viewer**.



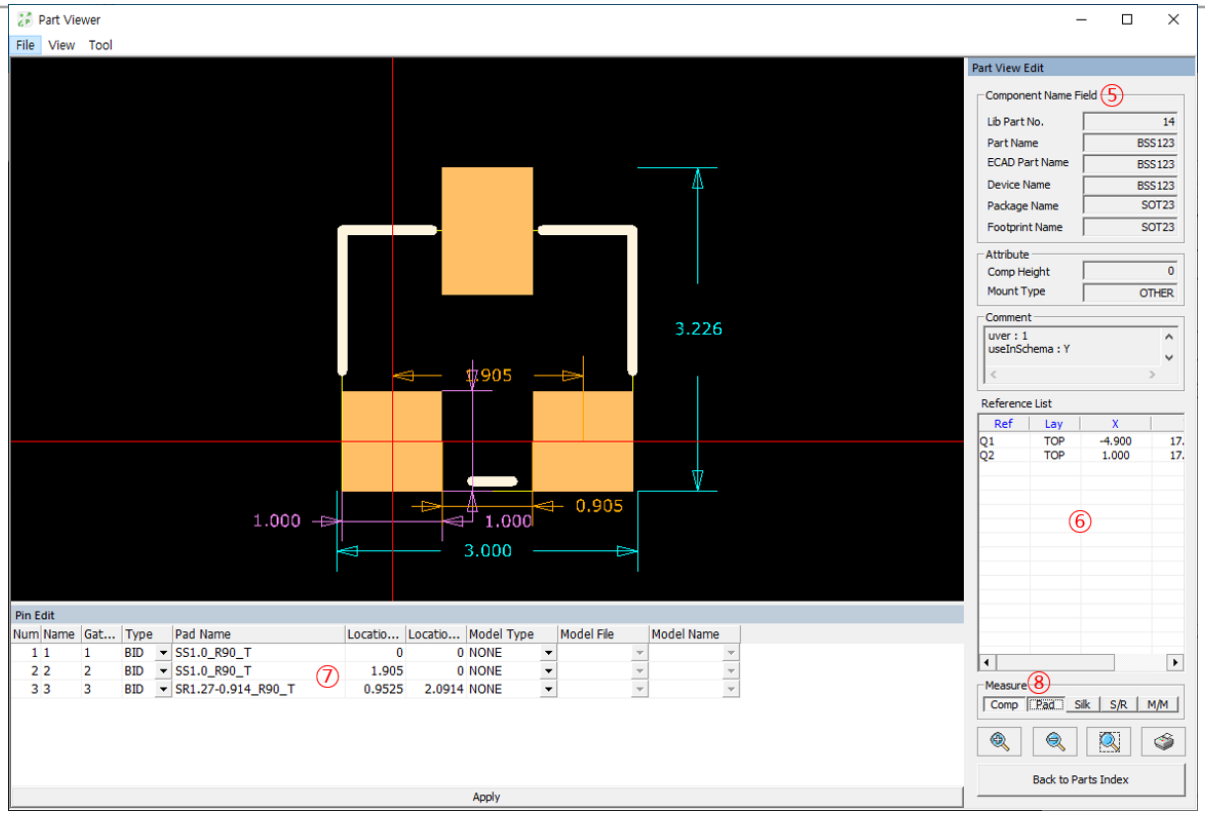
① At main window's left side, there is part's shape.

② At searching box, user can input keyword and find part.

③ At main window red line crossed point means origin points of part. User can change the origin of part.



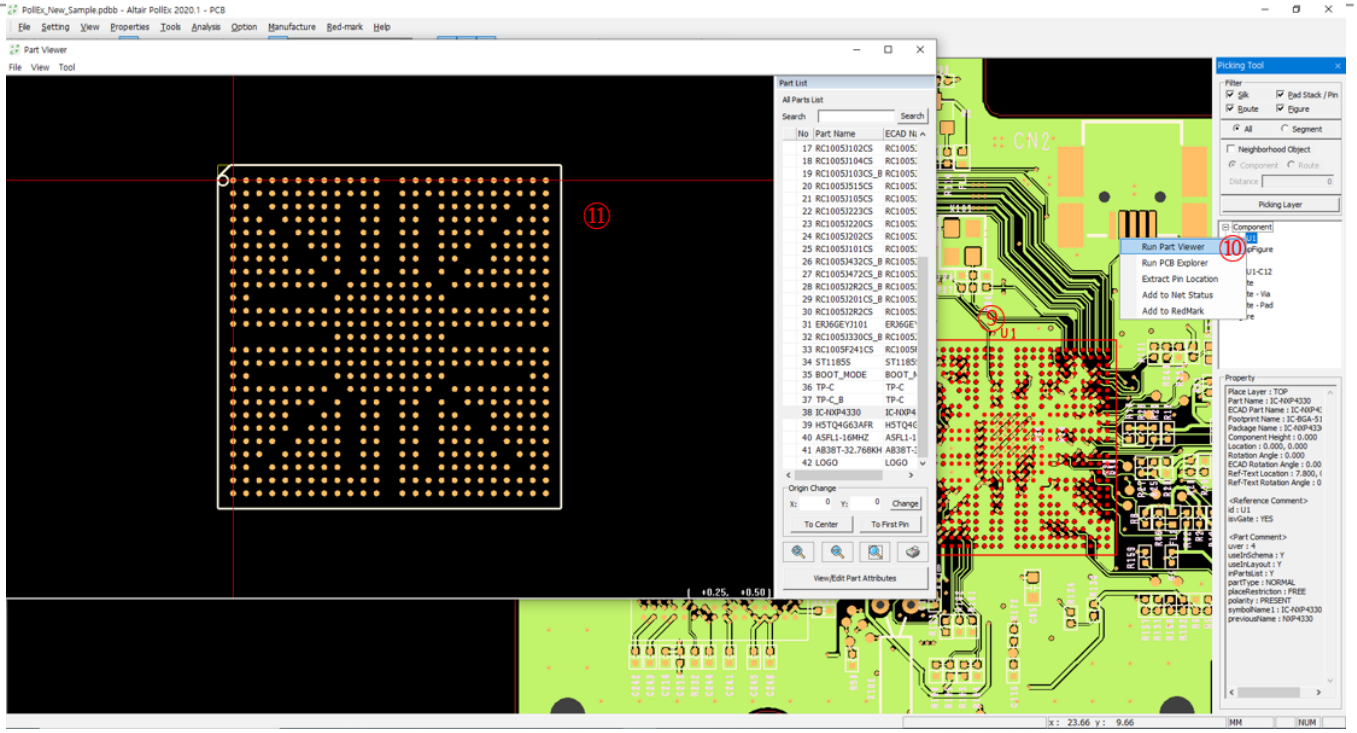
④ **View/Edit Part Attributes** button menu give users to check more detail information of part. After pressing this button, user can meet following picture's window.



⑤ **Component Name Field** contains different identifiers assign to part.
⑥ At this window, it shows referenced components list.
⑦ For pins used by part, this window shows whole properties of used pins.
⑧ Using various buttons in **Measure** tab, user can make displaying dimensions for component size, pad size, silk, solder/metal mask size.

※ Next is another way to invoke **Part Viewer** in other tools in PollEx PCB. Upon linking with other tools, user can use **Part Viewer** much easier.

1) Using **Part Viewer** in **Picking Tool**.

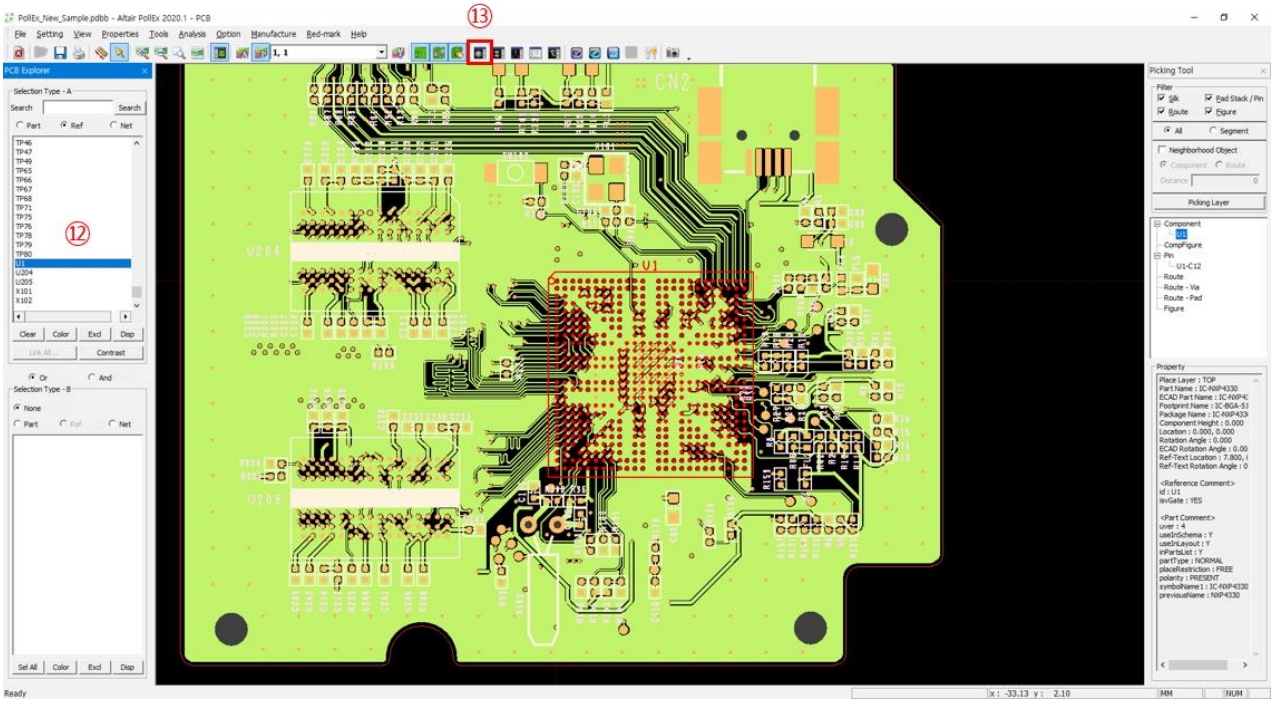


⑨ Upon launching picking tool, after selecting components list, using mouse right button, run a pop-up menu.

⑩ And, among the menus, select **Run Part Viewer.**

⑪ **Part Viewer** will be launched.

2) Using **Part Viewer** in **PCB Explorer**.



⑫ Upon launching **PCB Explorer**, at component list window, select component.

⑬ And use the menu, **Option > Part Viewer**. **Part Viewer** with selected part will be launched.

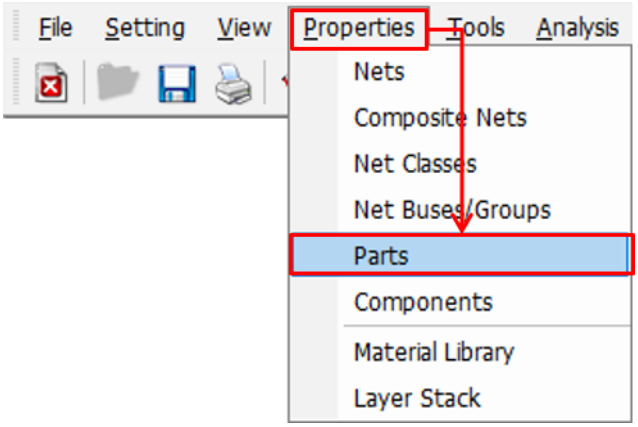
2. **Real PCB Assembly Viewer**

Real PCB Assembly Viewer connects the PCB design data and 3D UPF library to create 3D PCB shapes and export them as 3D common data like `*.stp` and `*.stl`.

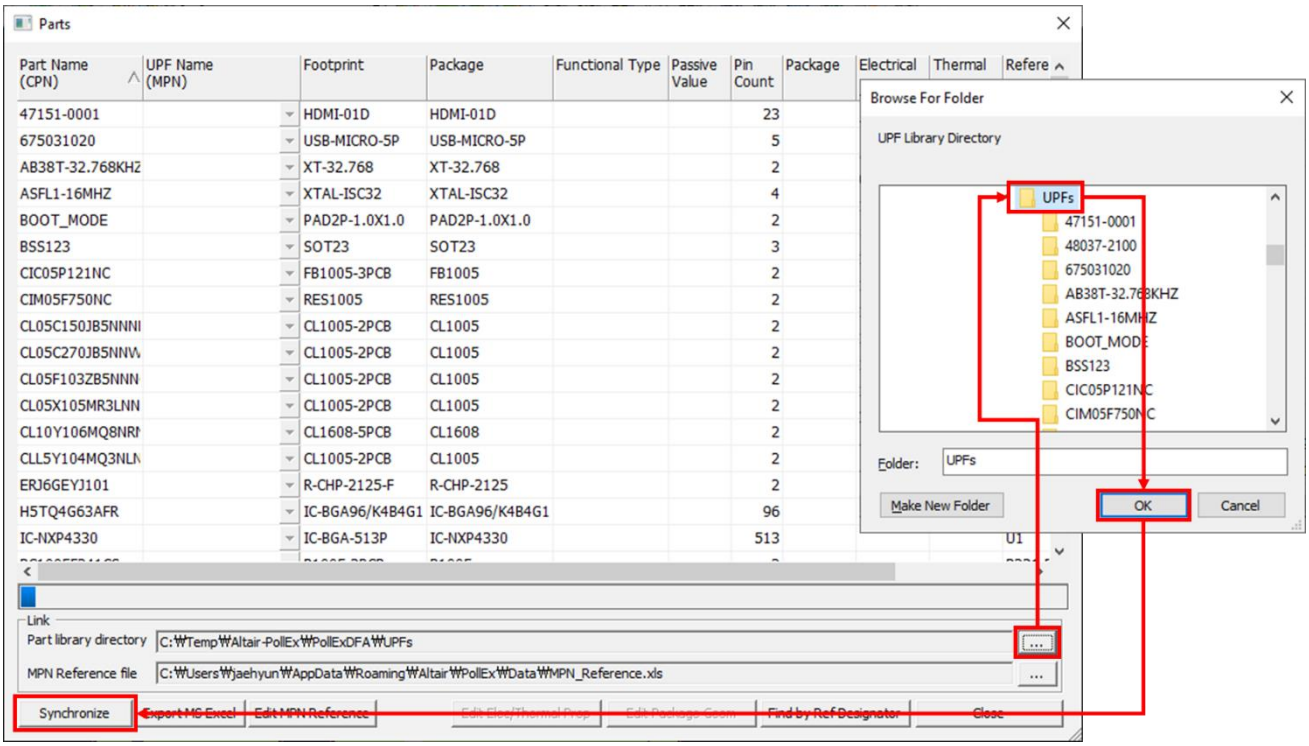
2.1. 3D UPF Library Link

Before using the Real PCB Assembly Viewer, users need to link 3D package libraries with PCB design.

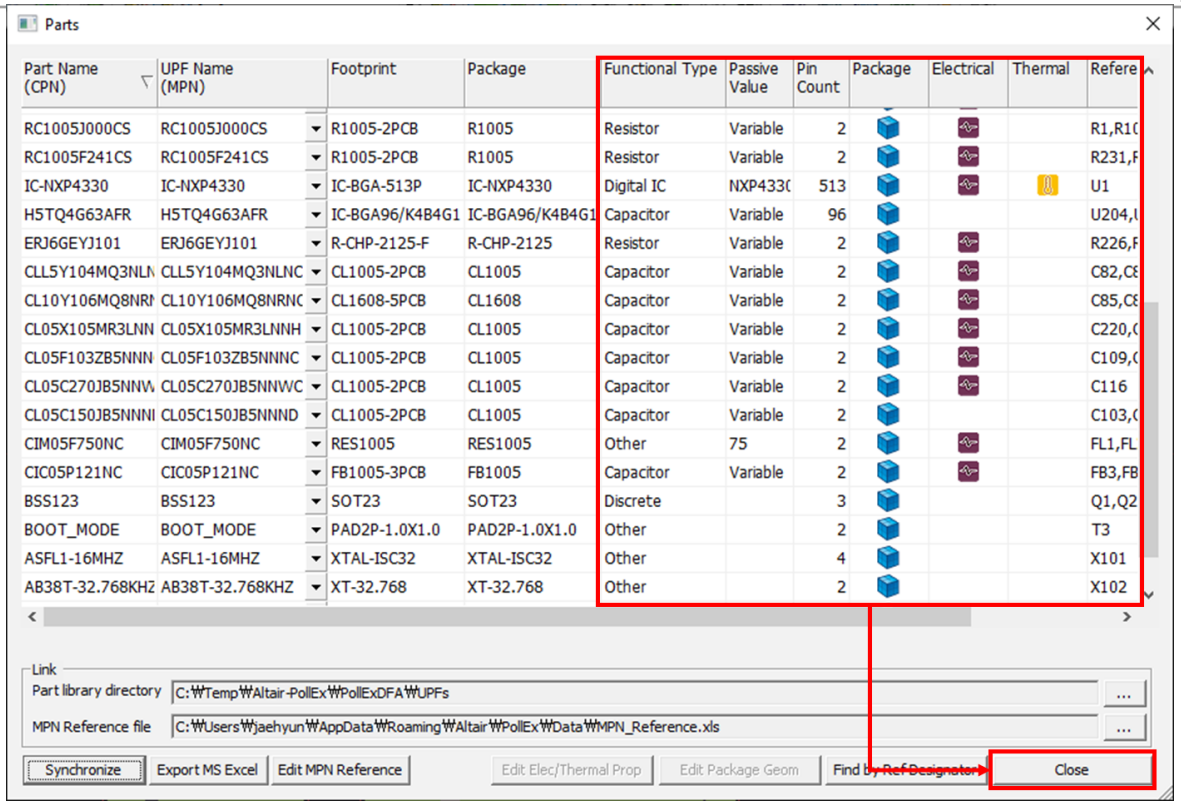
① Run **Properties > Parts** menu.



② Click the button "**...**" to set the UPF library path. If user sets the default part library directory in the environment setting (Setting > Environment > General), the user does not need to set it.

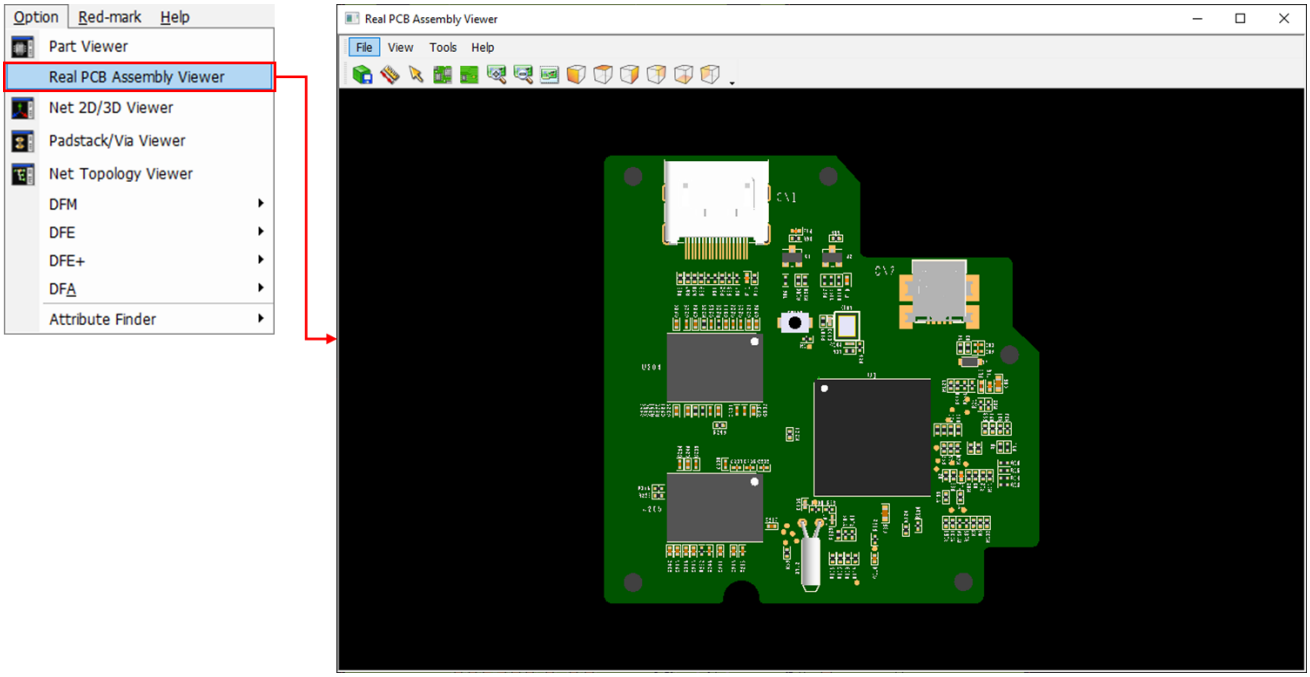


③ Click **Synchronize** button to display the UPF library setting information on each part. Click **Close** button to close the **Parts** dialog.

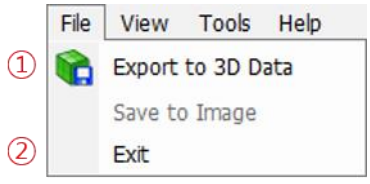


2.2. Real PCB Assembly Viewer

Run **Option > Real PCB Assembly Viewer** menu.



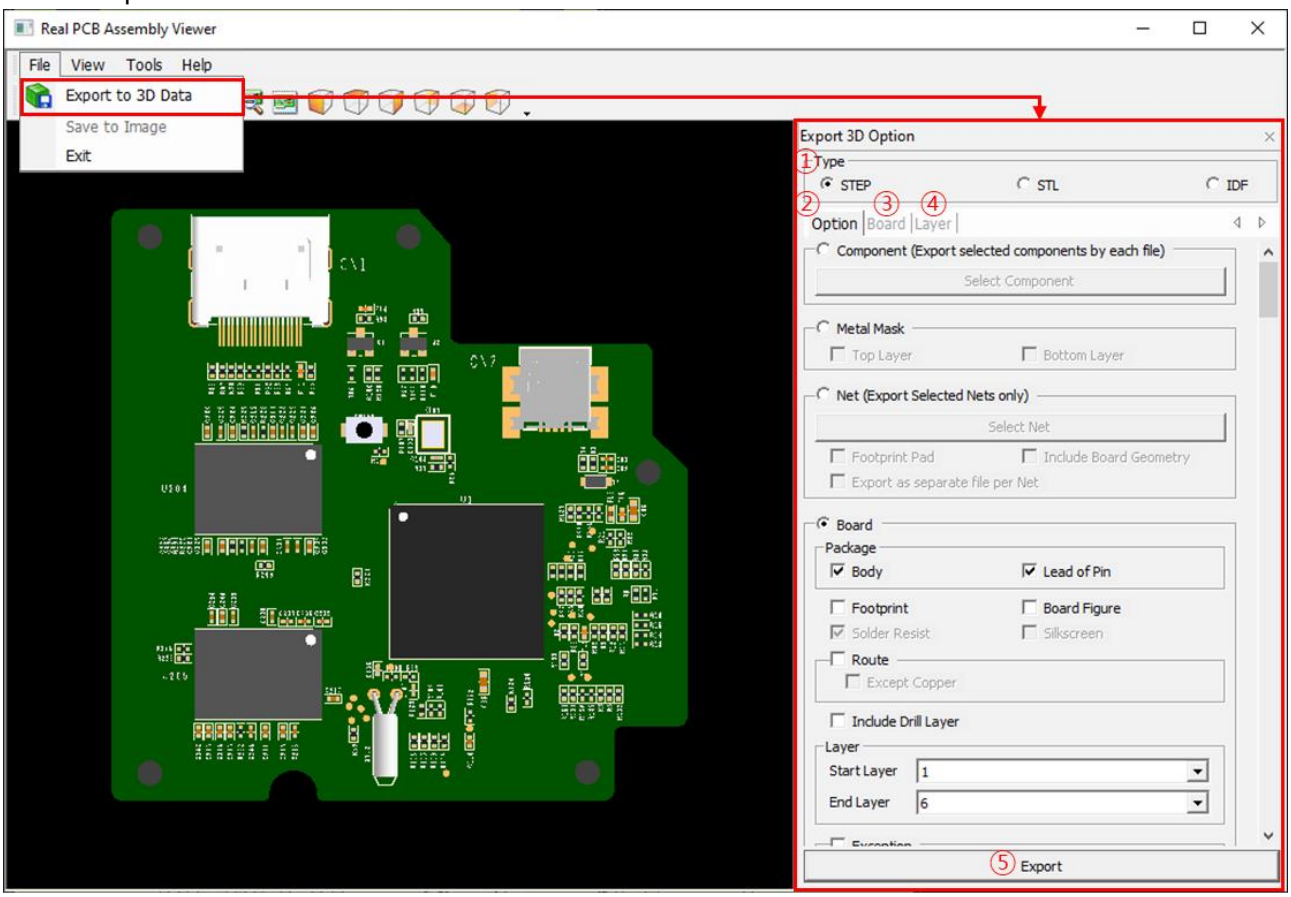
2.3. File



① Export to 3D Data
3D shaped PCB generated from the Real PCB Assembly Viewer can be exported to 3D common formats. Supported formats are `*.stp` and `*.stl`.

② Exit
Click Exit menu to close the Real PCB Assembly Viewer.

2.3.1. Export to 3D Data



Export to 3D Option

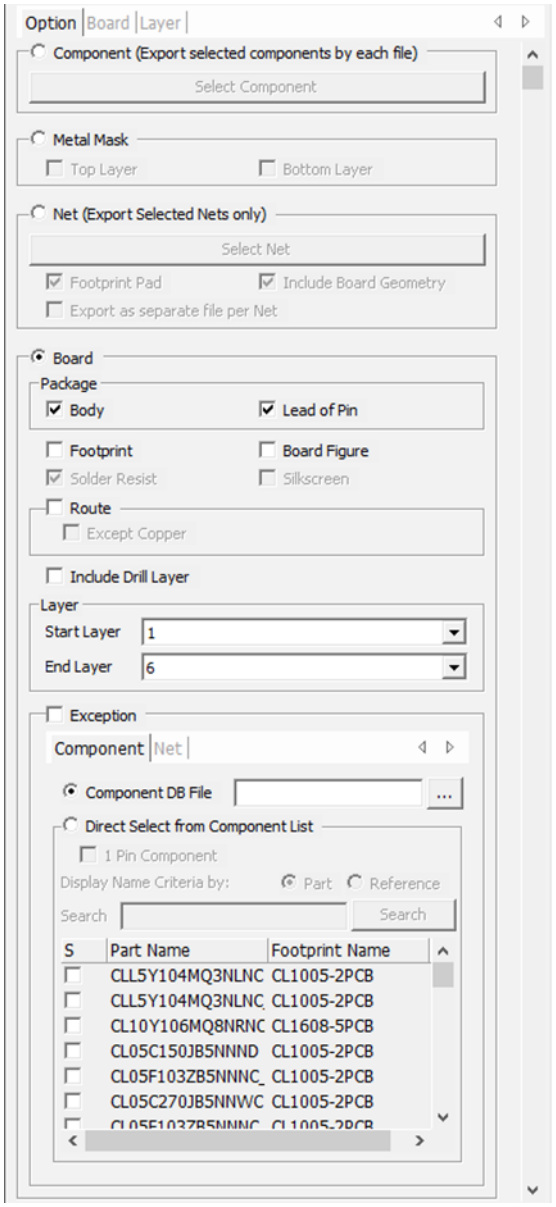
① Type
② Option
③ Board
④ Layer
⑤ Export

2.3.1.1. Type

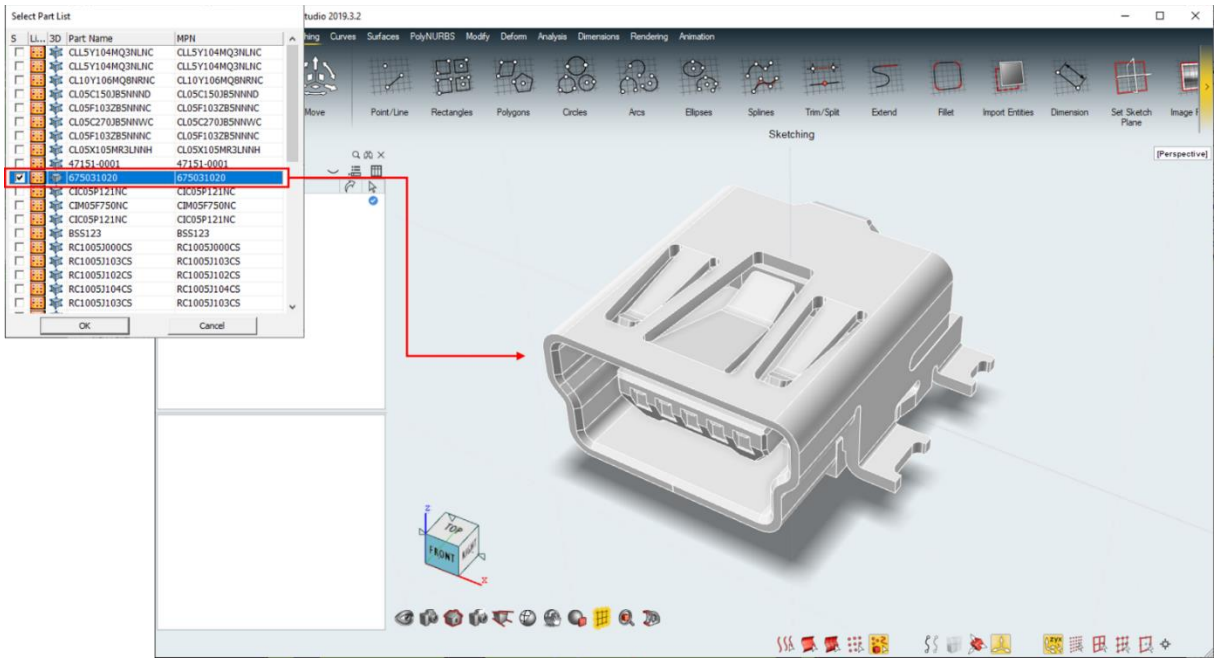
Specify the 3D data type to export.

2.3.1.2. Option

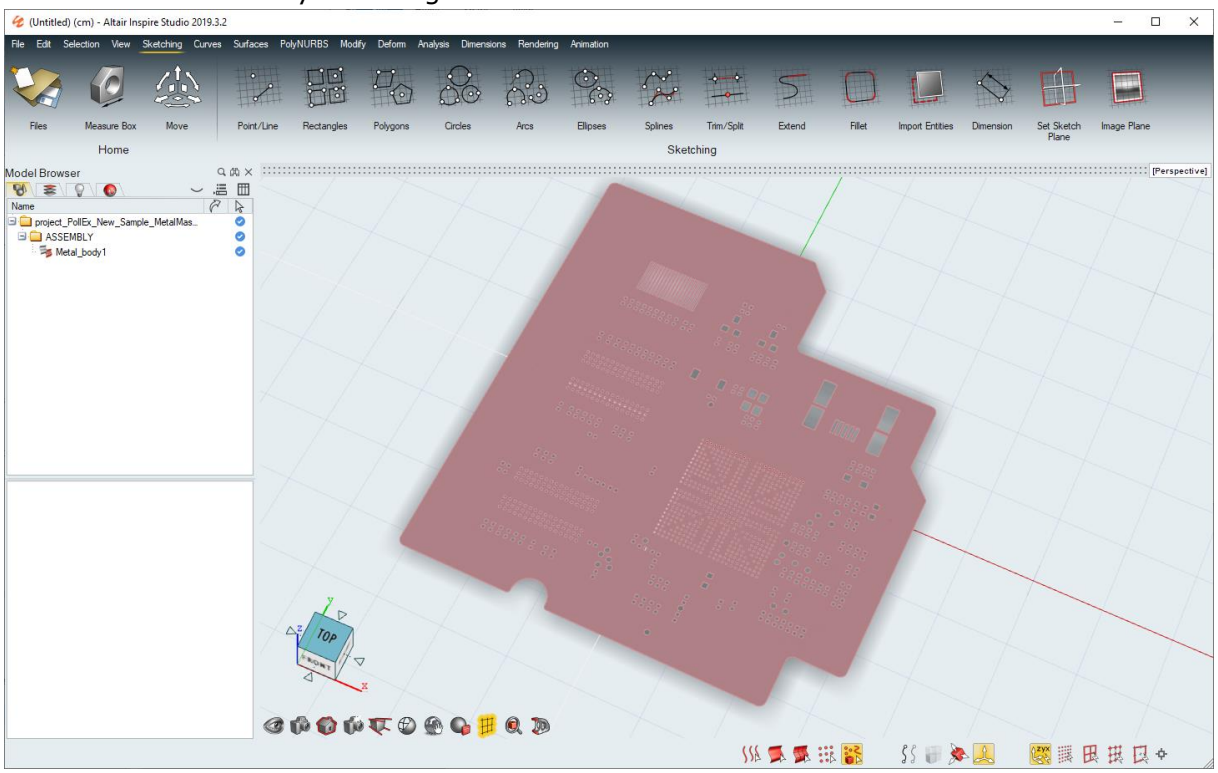
Set options for exporting as 3D data.



2.3.1.2.1. **Component (Export selected components by each file)**: Option to export the selected components used in the design data with 3D shape.



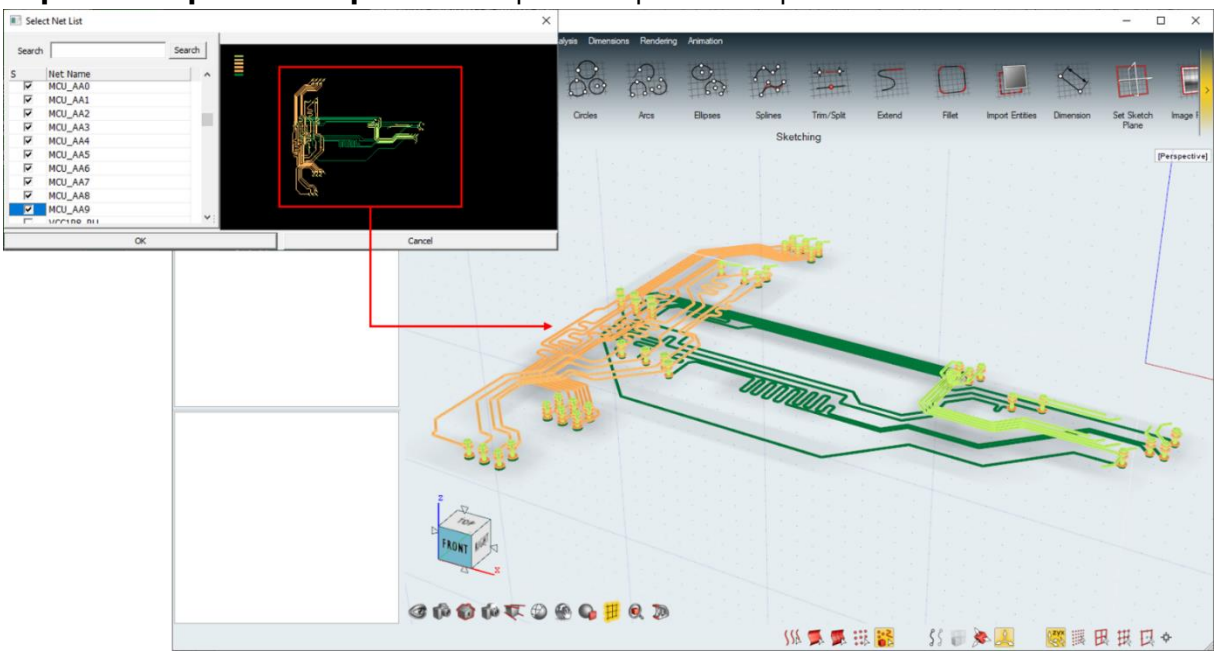
2.3.1.2.2. **Metal Mask**: Metal Mask drawn as positive on the PCB design data is converted into negative and exported as 3D data. User should set the Metal Mask thickness in the layer setting.



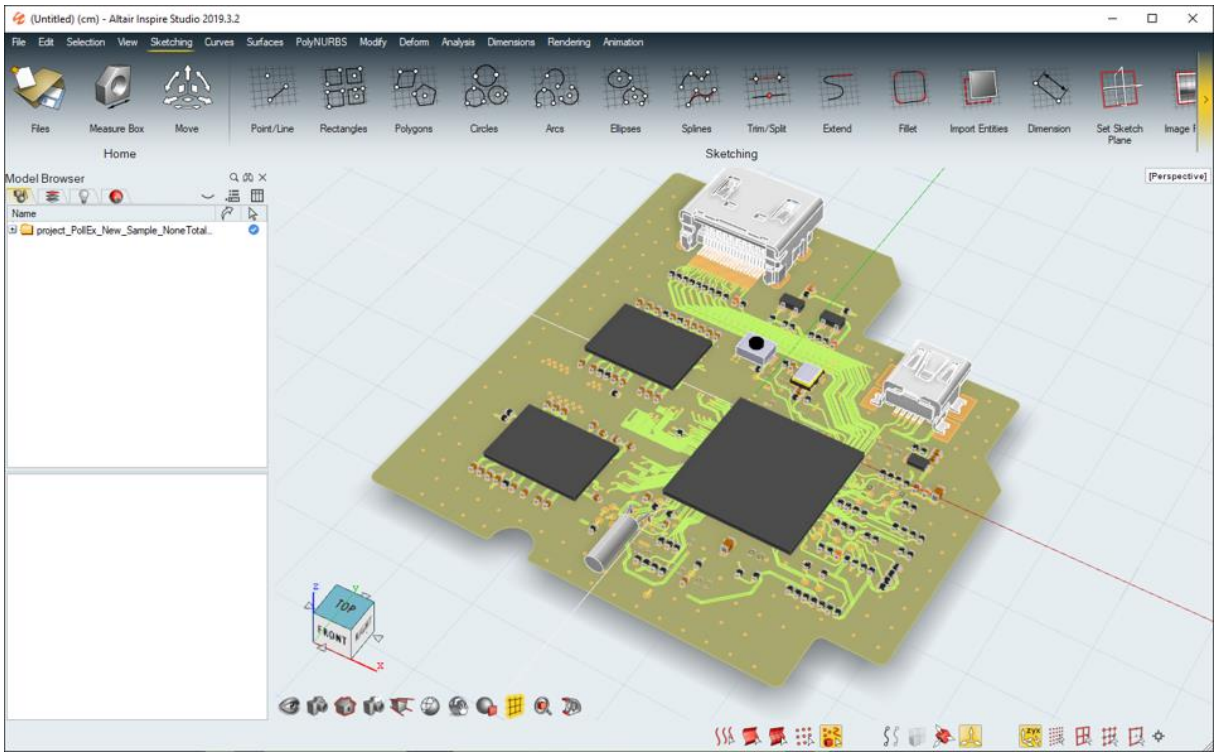
2.3.1.2.3. **Net(Export Selected Nets only)**: Option to export the selected Net as 3D data.

- **Footprint Pad**: Export including the footprint pad which connected to the net.
- **Include Board Geometry**: Export including the PCB board shape.

- **Export as separate file per Net**: Export a separate file per a net.



2.3.1.2.4. **Board**: Option to export the shapes of the board and components in the design data.



-. Package: Select whether to export package **Body** and **Lead of Pin**.
-. Footprint: Select whether to export part footprint.
-. Board Figure: Select whether to export the board figure drawing in the PDB design data.
-. Solder Resist: Select whether to export the solder resist.
-. Silkscreen: Select whether to export the silkscreen.
-. Route: Select whether to export the routing.
Except Copper: Option to exclude the copper-pour.

-. Include Drill Layer: Select whether to export the shape of drill properties like through hole, via hole and figure hole.

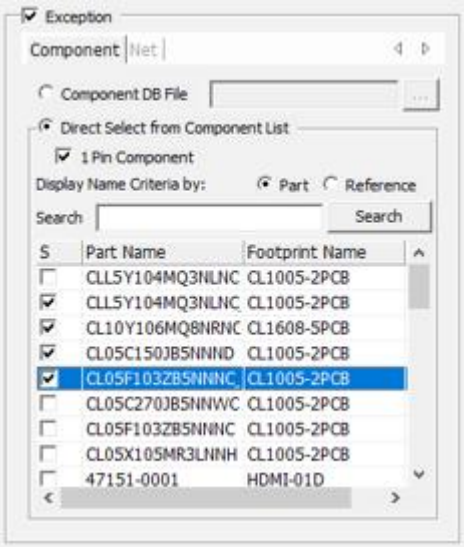
-. Layer: Set the range of layers to be exported.

Start Layer: Set the start layer.

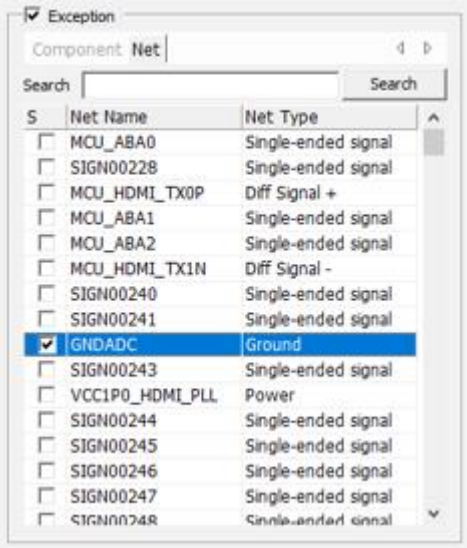
End Layer: Set the end layer.

-. Exception: Option to exclude components and nets.

Component: Select the components to be excluded from the list or use the Component DB(`*.txt`) file.

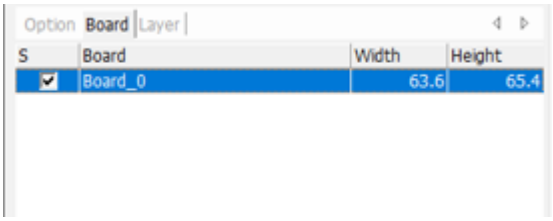


Net: Select the nets to be excluded from the list.



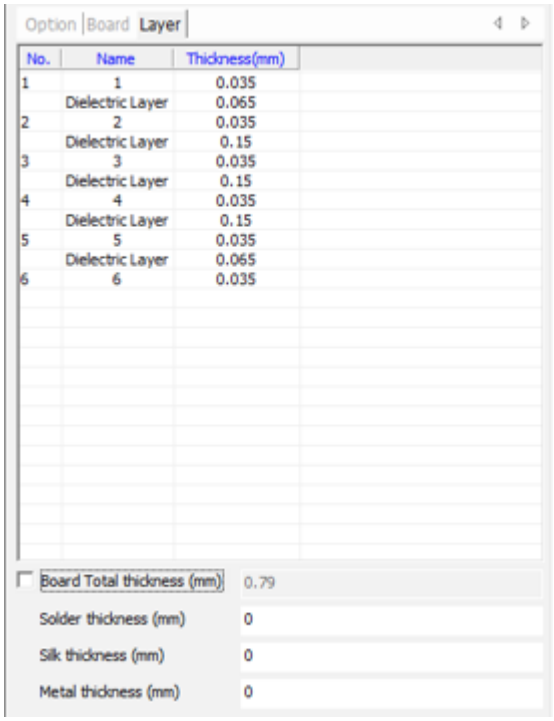
2.3.1.3. Board

Select the board to export from the list if there are multiple boards in the PCB design data like the Panel PCB.



2.3.1.4. Layer

Set the thickness of the PCB board.



-. Table

No.: Display the physical layer number.

Name: Display the layer name.

Thickness(mm): Display the thickness of the layer. The displayed value can be modified by double-clicking it.

-. Board Total thickness(mm): If checked this option, the thickness of layers specified above is ignored and user can define the total thickness of the board.

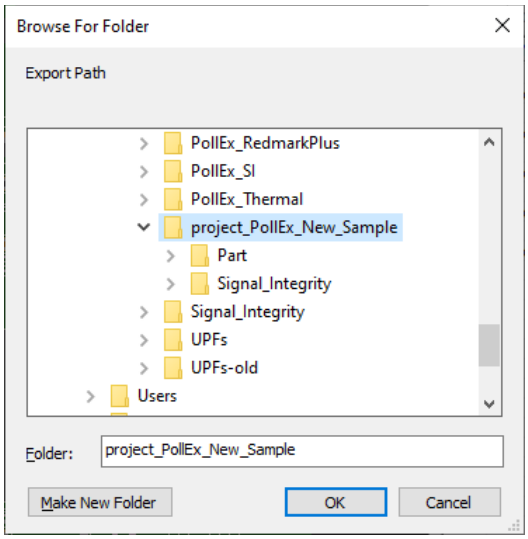
Solder thickness (mm): Set the thickness of the solder resist.

Silk thickness (mm): Set the thickness of the silk.

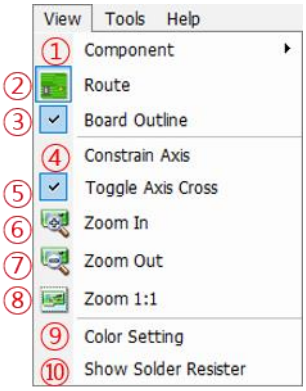
Metal thickness (mm): Set the thickness of the metal mask.

2.3.1.5. Export

Set the export path.

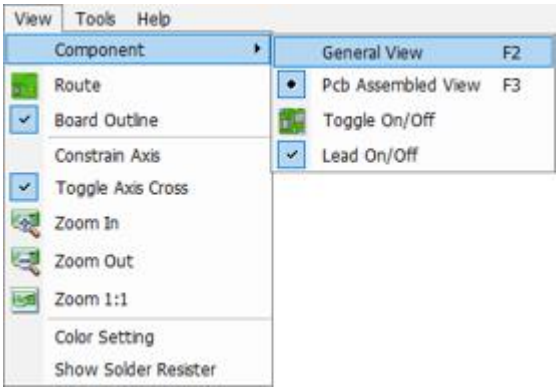


2.4. View

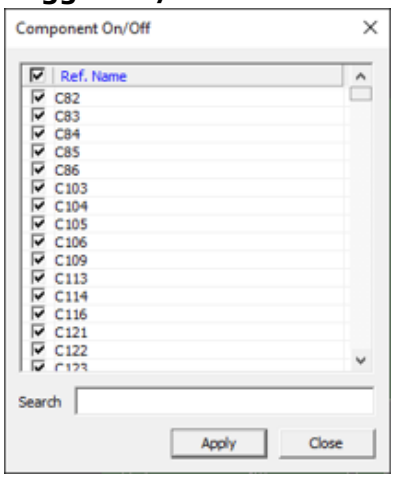


① Component
② Route
③ Board Outline
④ Constrain Axis
⑤ Toggle Axis Cross
⑥ Zoom In
⑦ Zoom Out
⑧ Zoom 1:1
⑨ Color Setting
⑩ Show Solder Resist

2.4.1. Component



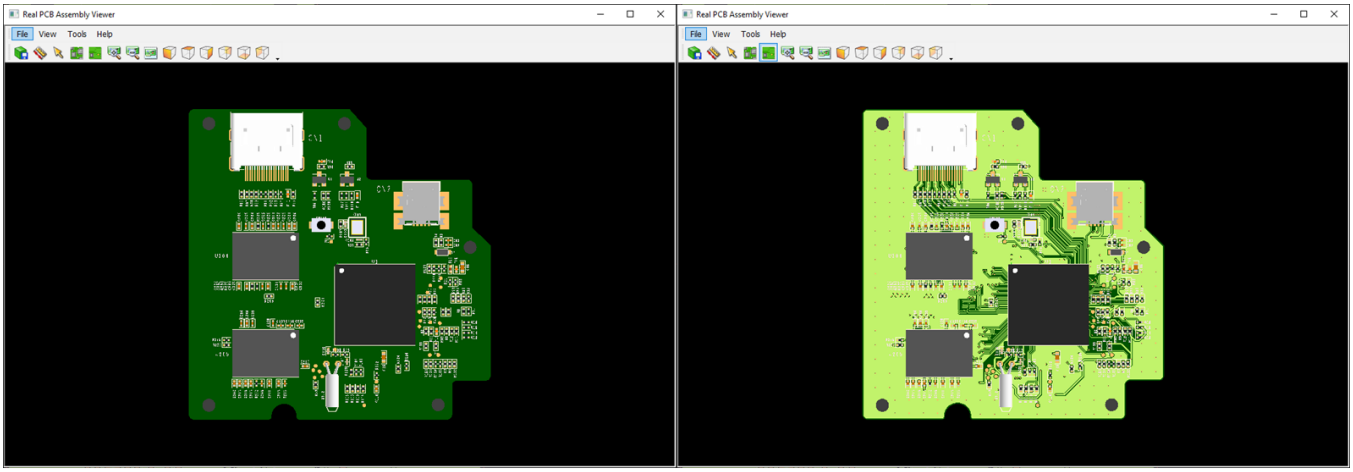
① **General View**: Display only PCB shape except 3D components.
② **PCB Assembled View**: Display both PCB shape and 3D components.
③ **Toggle On/Off**: Select whether to display per component reference in the list.



④ **Lead On/Off**: Select whether to display the component lead.

2.4.2. Route

Option to turn on or off the 3D PCB geometry.

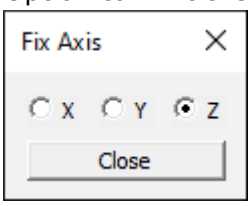


Route Display Off Route Display On

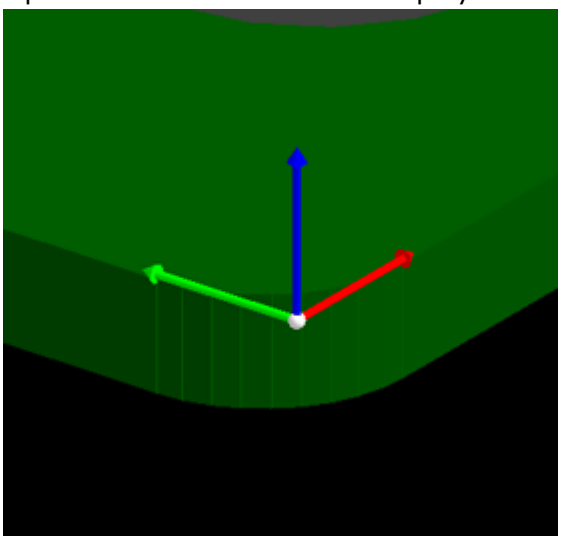
2.4.3. Board Outline

Option to turn on or off the board outline display, only when the width value is drawn more than 0.

2.4.4. Constrain Axis
Option to limit the rotation axis.



2.4.5. Toggle Axis Cross
Option to turn on or off the display of XYZ axis pivot.

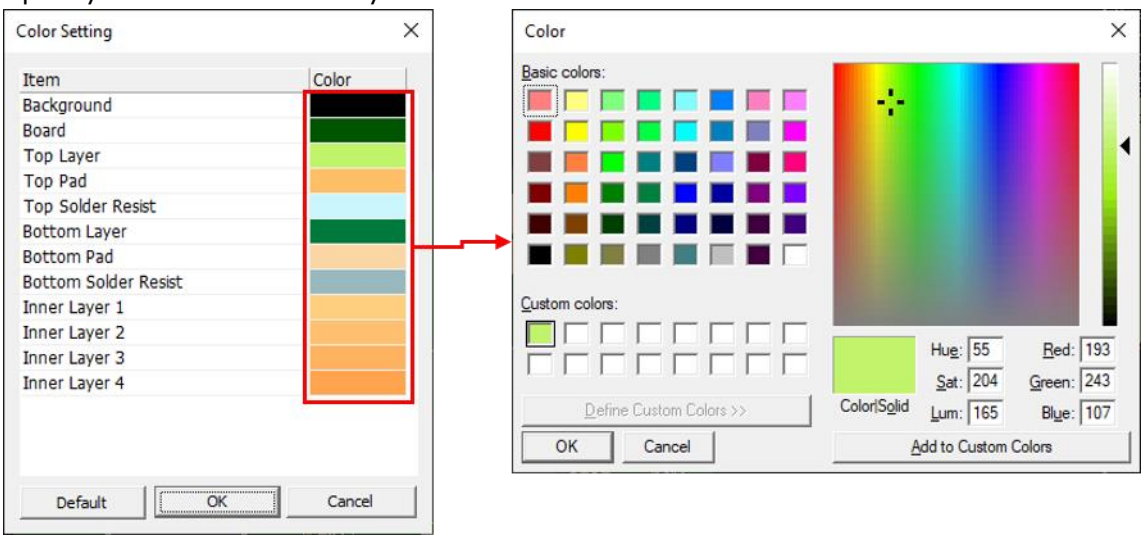


2.4.6. Zoom In/Out
Option to zoom in or out.

2.4.7. Zoom 1:1
Restore the display to default.

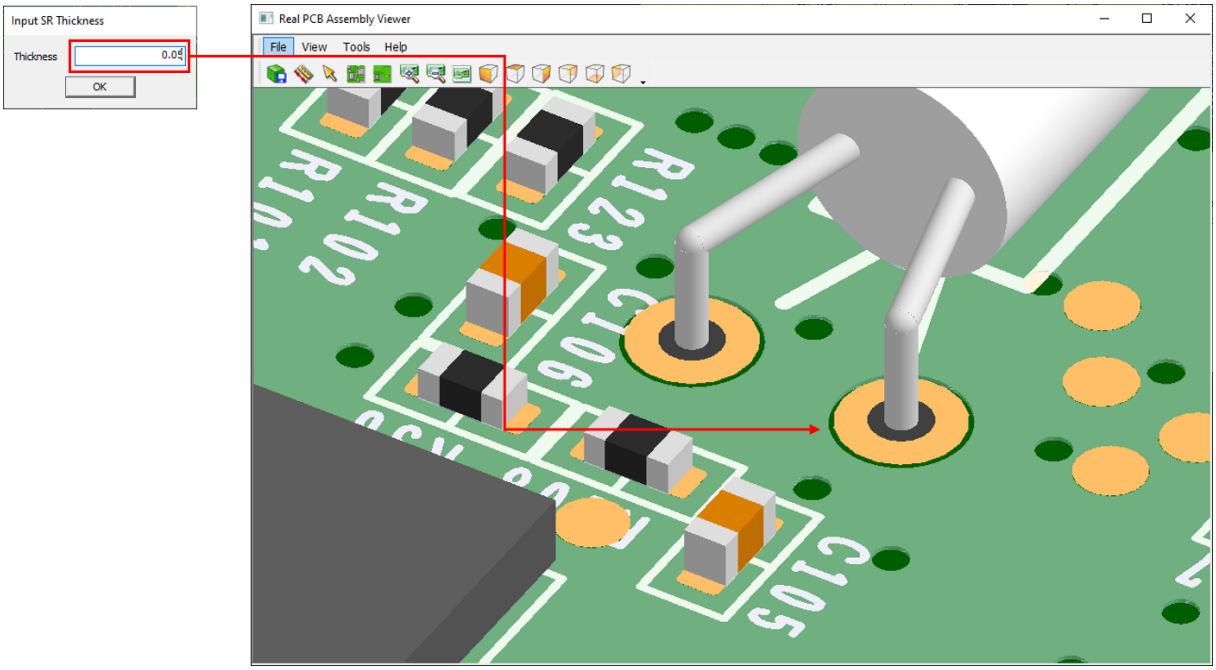
2.4.8. Color Setting

Specify the color of each layer.



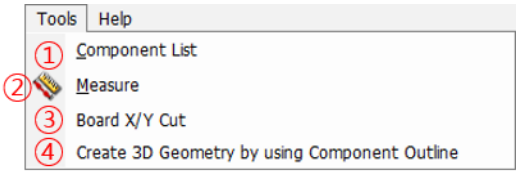
2.4.9. Show Solder Resist

The solder mask designed as positive in PCB design data is converted to negative to display the solder resist layer as much as the input thickness.



2.5. Tools

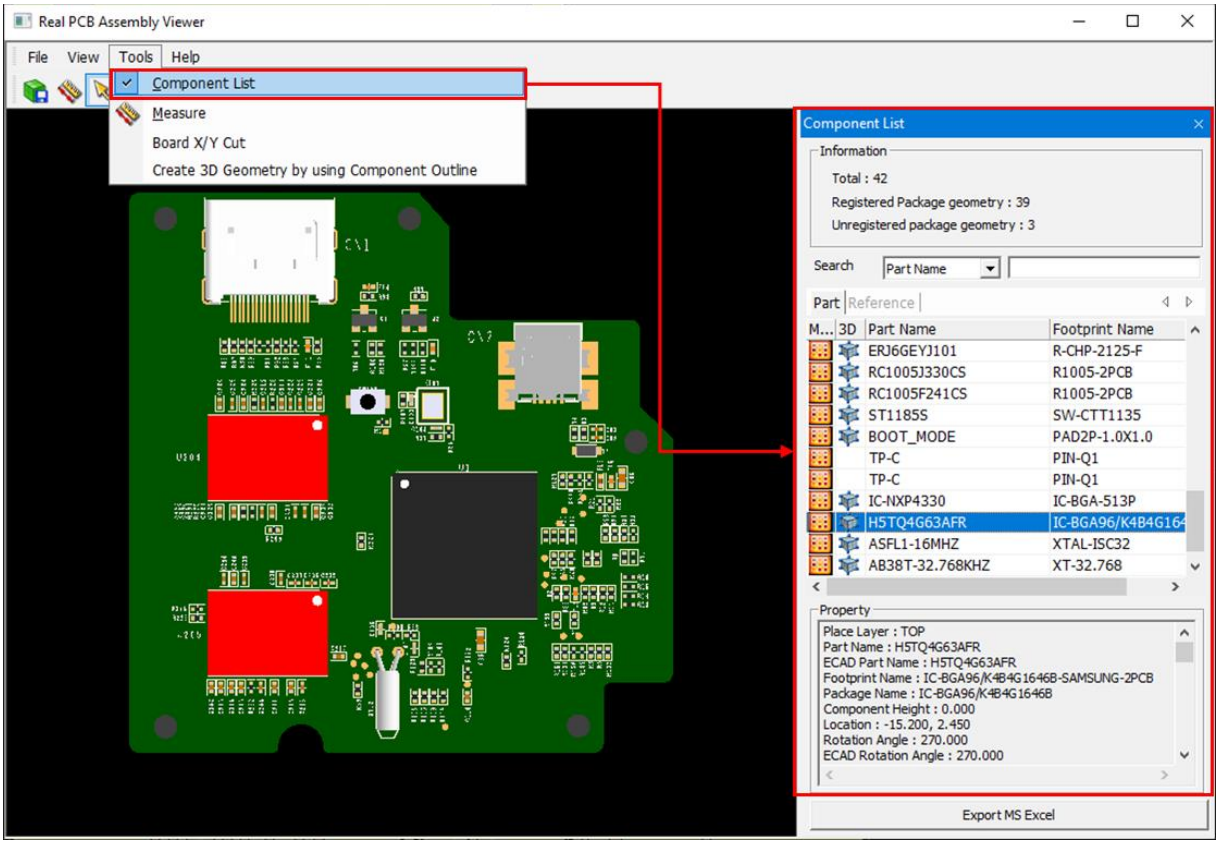
This item provides convenient functions such as measuring distance between parts and cutting board view.



① Component List
② Measure
③ Board X/Y Cut
④ Create 3D Geometry by using Component Outline

2.5.1. Component List

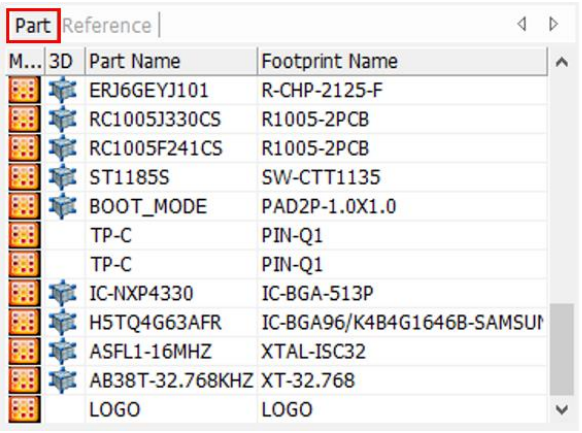
Search the parts used in the design.

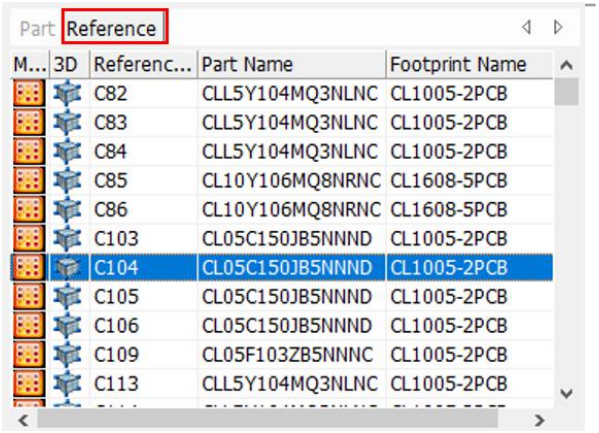


2.5.1.1. Information: Export information of components in the PCB design.

① **Total**: The total number of components used in the PCB design.
② **Registered package geometry**: The number of components with the 3D geometry registered in the UPE library.
③ **Unregistered package geometry**: The number of components with the 3D geometry not registered in the UPE library.
④ **Search**: Search components by Part Name or Reference Name.

2.5.1.2. Part/Reference Table: List of components used in the PCB design can be checked the information. The component is highlighted in red when selected a component from the list.

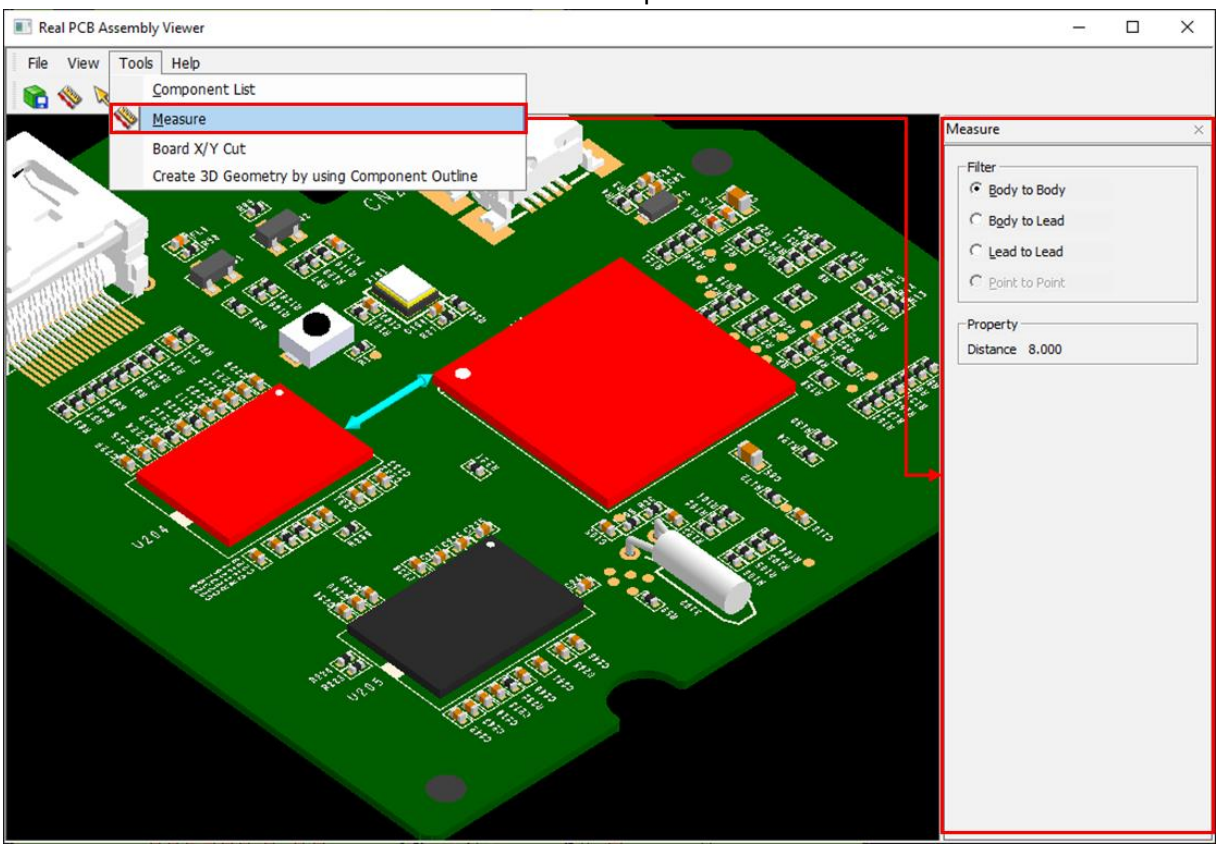




2.5.1.3. Property: Check the property information of selected component.

2.5.2. Measure

This menu measures the distance between components.



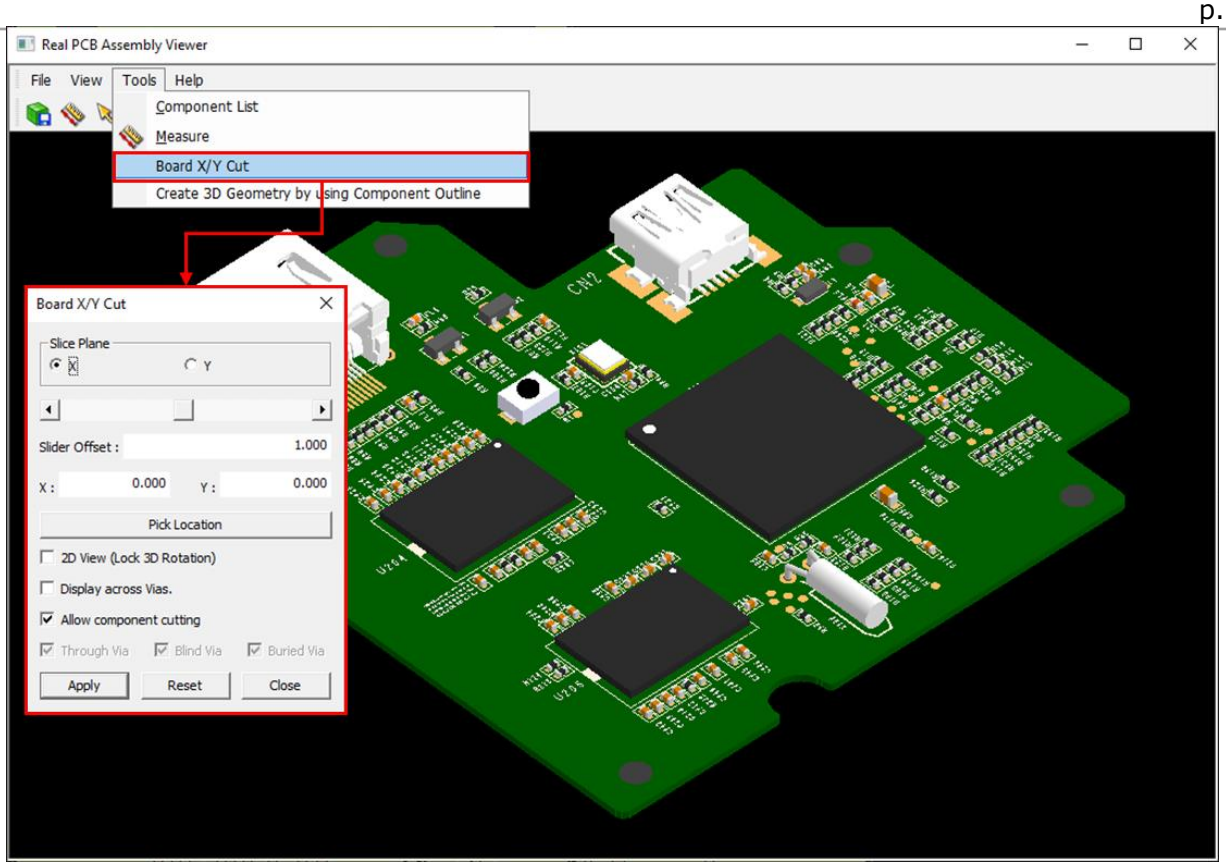
① **Body to Body**: Measure the closest distance between the bodies. The measured value can be checked in **Property**.

② **Body to Lead**: Measure the closest distance between the body and lead. The measured value can be checked in **Property**.

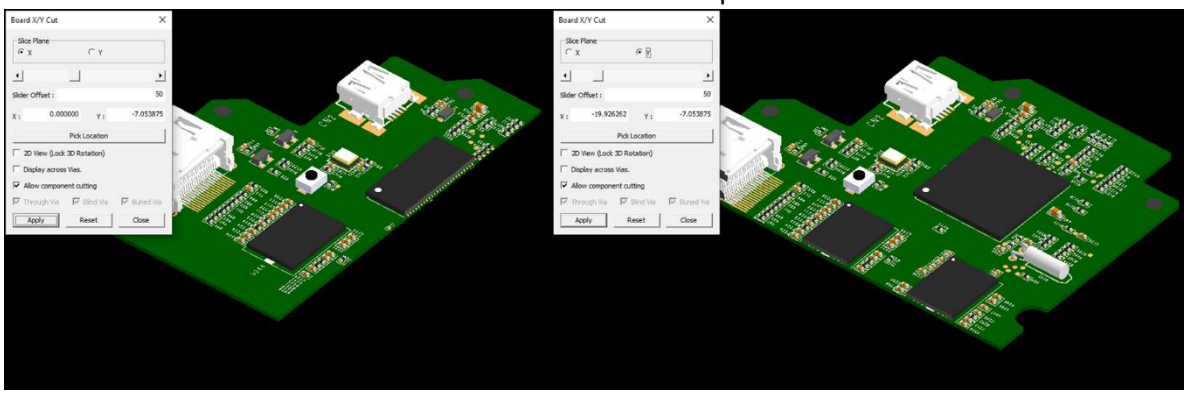
③ **Lead to Lead**: Measure the closest distance between the leads. The measured value can be checked in **Property**.

2.5.3. Board X/Y Cut

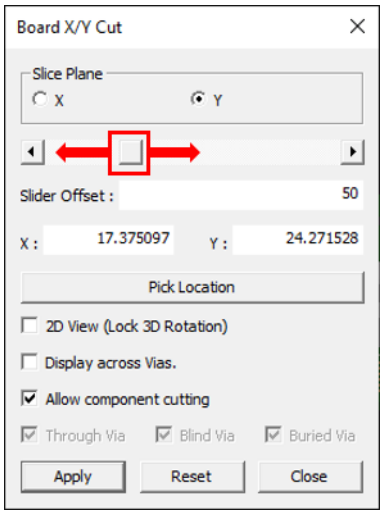
Check the PCB cutting surface.



2.5.3.1. Slice Plane: Select the X or Y axis of the cut plane.



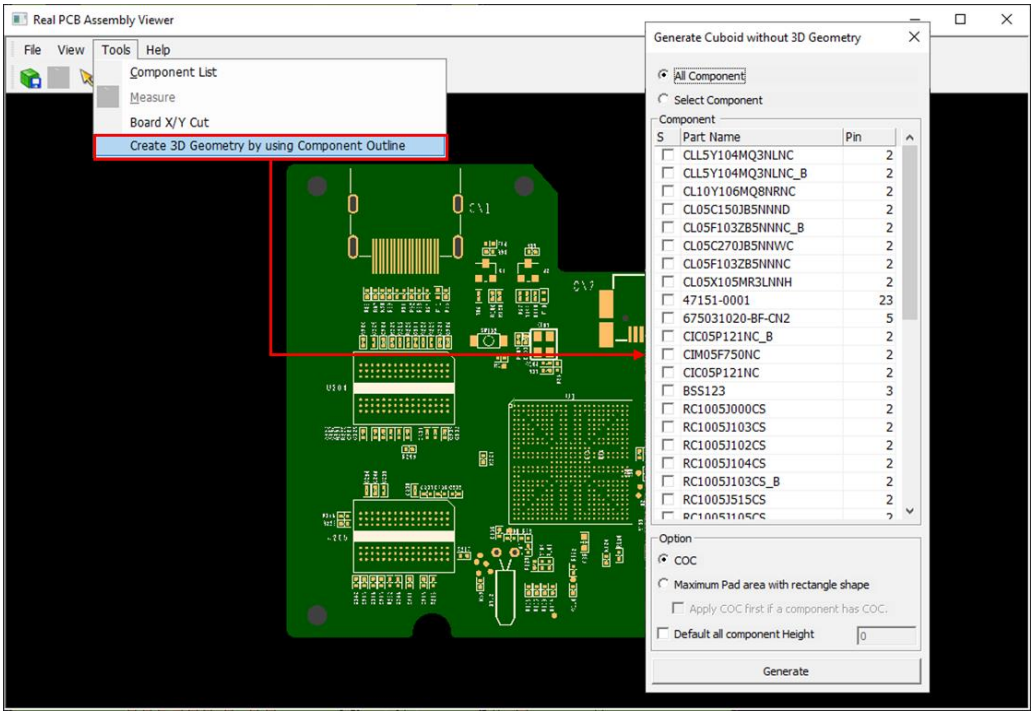
2.5.3.2. Scroll: Move the selected cutting plane by moving the slider scroll.



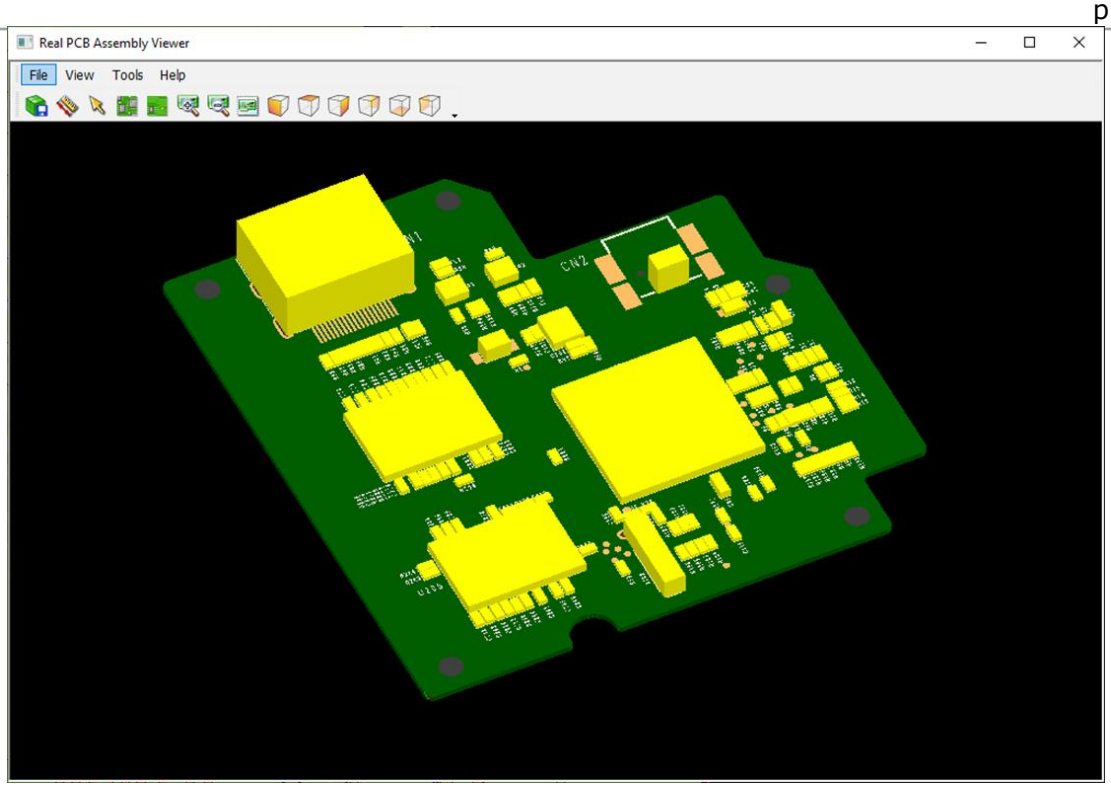
① **Slider Offset**: Slide bar moves by the Slider Offset value.
② **X**, **Y**: Indicate the X, Y coordinates of the cutting plane.
③ **Pick Location**: Specify the cutting plane location by clicking the desired location.
④ **2D View (Lock 3D Rotation)**: Display the cutting surface in 2D.
⑤ **Display across Vias**: Select whether to display Vias in the cutting plane.
⑥ **Allow component cutting**: Select whether to cut the component.
⑦ **Through Via**, **Blind Via**, **Buried Via**: Select whether to display per via type.

2.5.4. Create 3D Geometry by using Component Outline

3D geometry is created by using the COC shape and height information of the component if there is no 3D UPF library.



① **All Component**: Generate 3D geometry for all components in the PCB.
② **Select Component**: Generate 3D geometry for the selected components from the list.



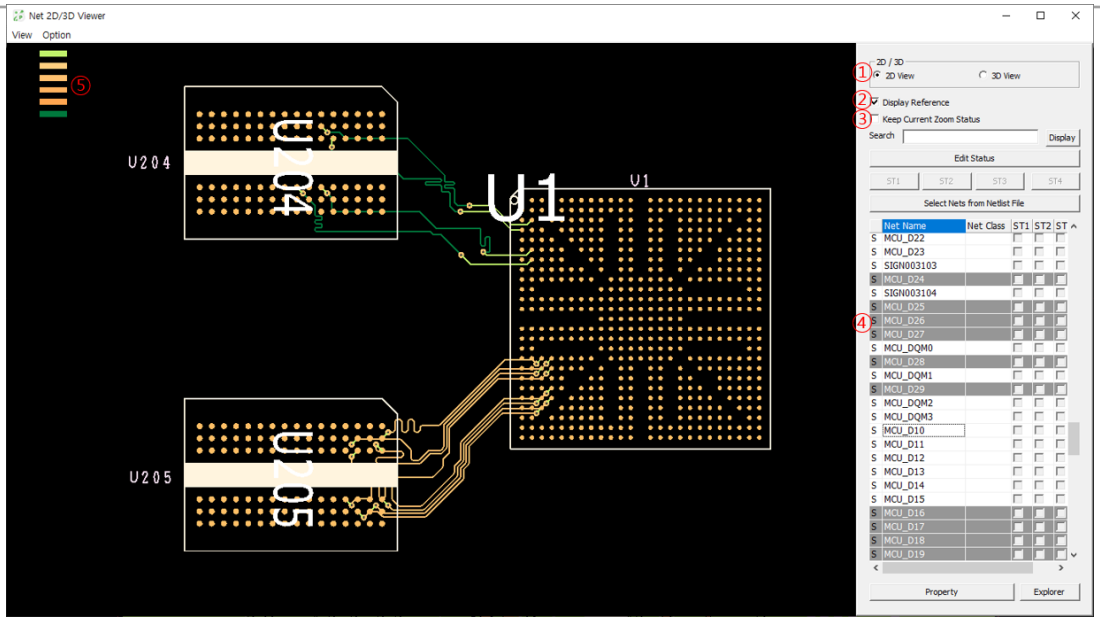
③ **Option**: Option to generate 3D part shape.
- **COC**: 3D part shape is created based on the component boundary of the footprint.
- **Maximum Pad area with rectangle shape**: 3D part shape is created based on the largest rectangular area of the footprint pad.
  - **Apply COC first if a component has COC.**: If a part has a COC (component boundary), 3D part shape is created based on the component boundary of the footprint first. The rest parts which do not have the COC will be created the 3D part shape based on the largest rectangular area of the footprint pad.
- **Default all component Height**: 3D part shape is created the height of all parts with the entered value.

3. **Net 2D/3D Viewer**

Net 2D/3D Viewer is viewer for reviewing routing nets on PCB. For net structure, it shows structure with 2D or 3D mode. It also supports for multiple nets. Use the menu, **Option > Net 2D/3D Viewer**.

3.1. Multiple Net Selection

Ctrl + Select Net



<Net 2D viewer>

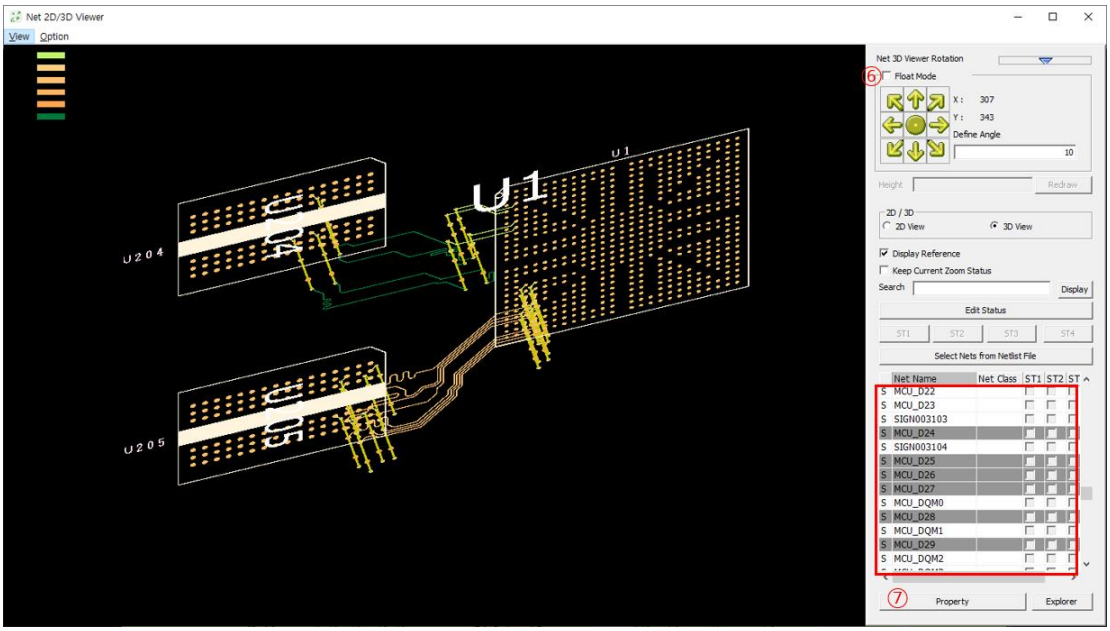
① Net displaying mode. Select on between **2D View** and **3D View**.

② Display Reference Name.

③ When user select a net in the list, the zoom status changes according to the net size. if this option is checked, current zoom status will not be changed. But the selected nets will be displayed to that screen.

④ Net selection window. Select target net(s).

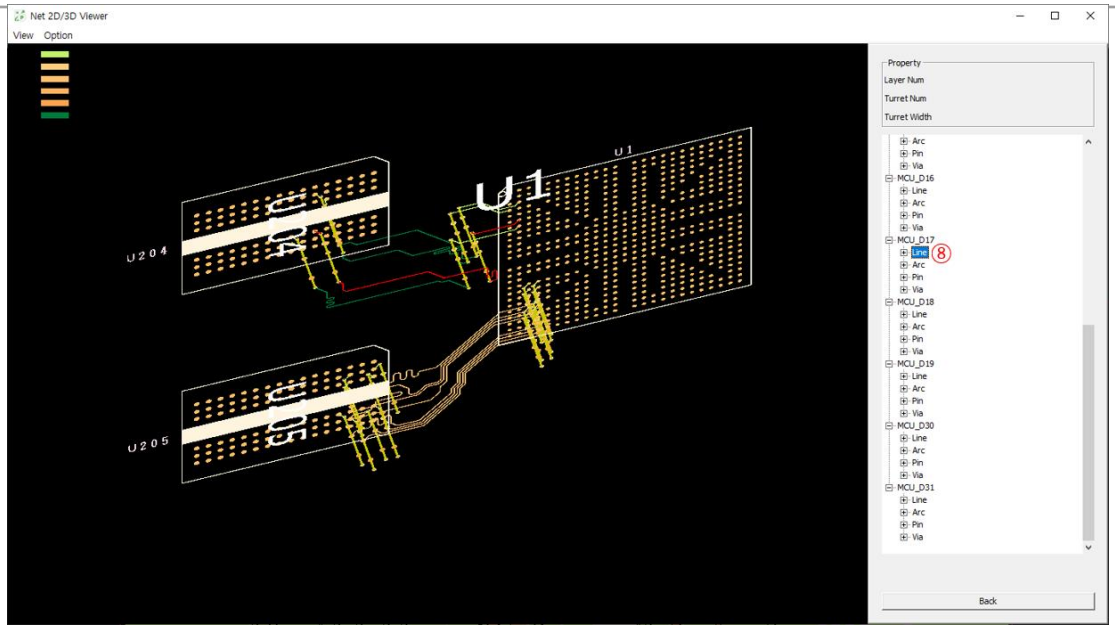
⑤ Color table for showing each physical layer's color.



<Net 3D viewer>

⑥ Rotation Control in 3D viewing mode.

⑦ **Property** button will show much detail information for selected net. At new dialog tab, user can see via's location, pattern segment or other net construction structure.

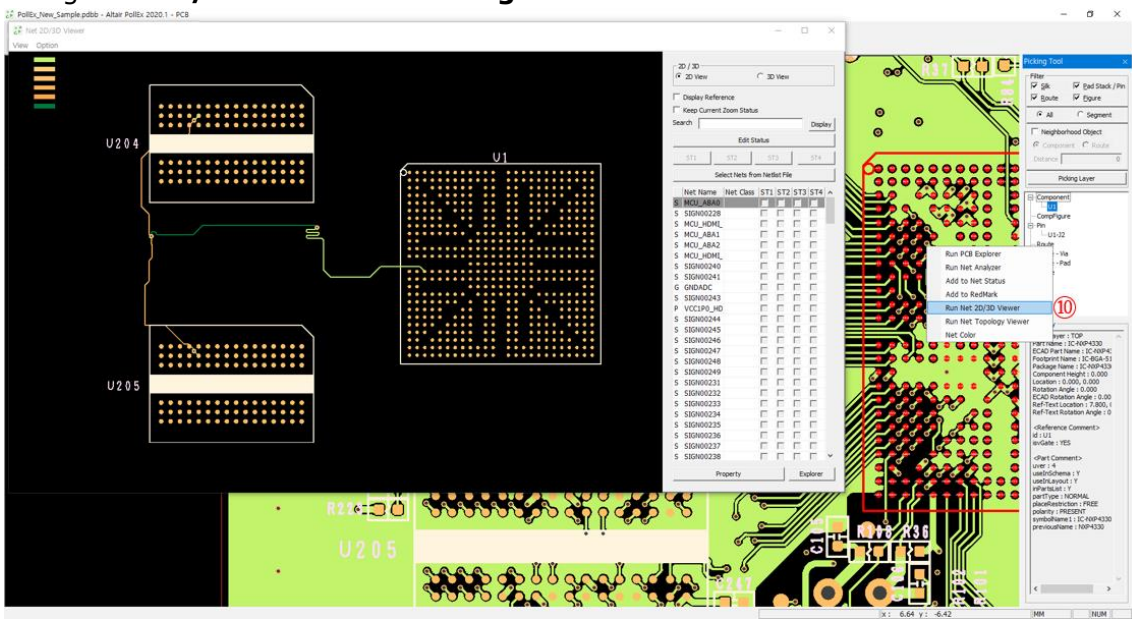


<Net Property>

⑧ **Property** tab contains hierarchical net structure.

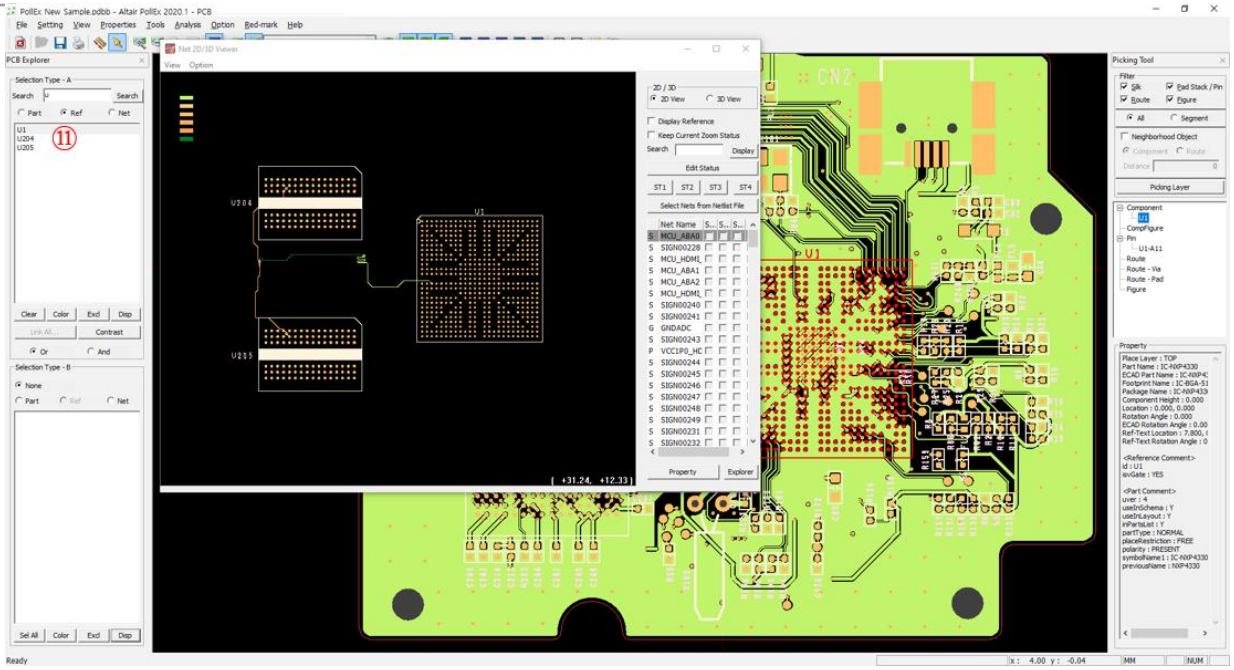
⑨ At property dialog tab, user can see detain information. At picture user can check the accurate pin location, component name and pin number.

⑩ Using **Net 2D/3D Viewer** in **Picking Tool**.



Upon launching picking tool, after selecting net among list, using mouse right button, run a pop-up menu. Among pop-up menu list, select **Net 2D/3D Viewer**. It will launch viewer for selected net(s).

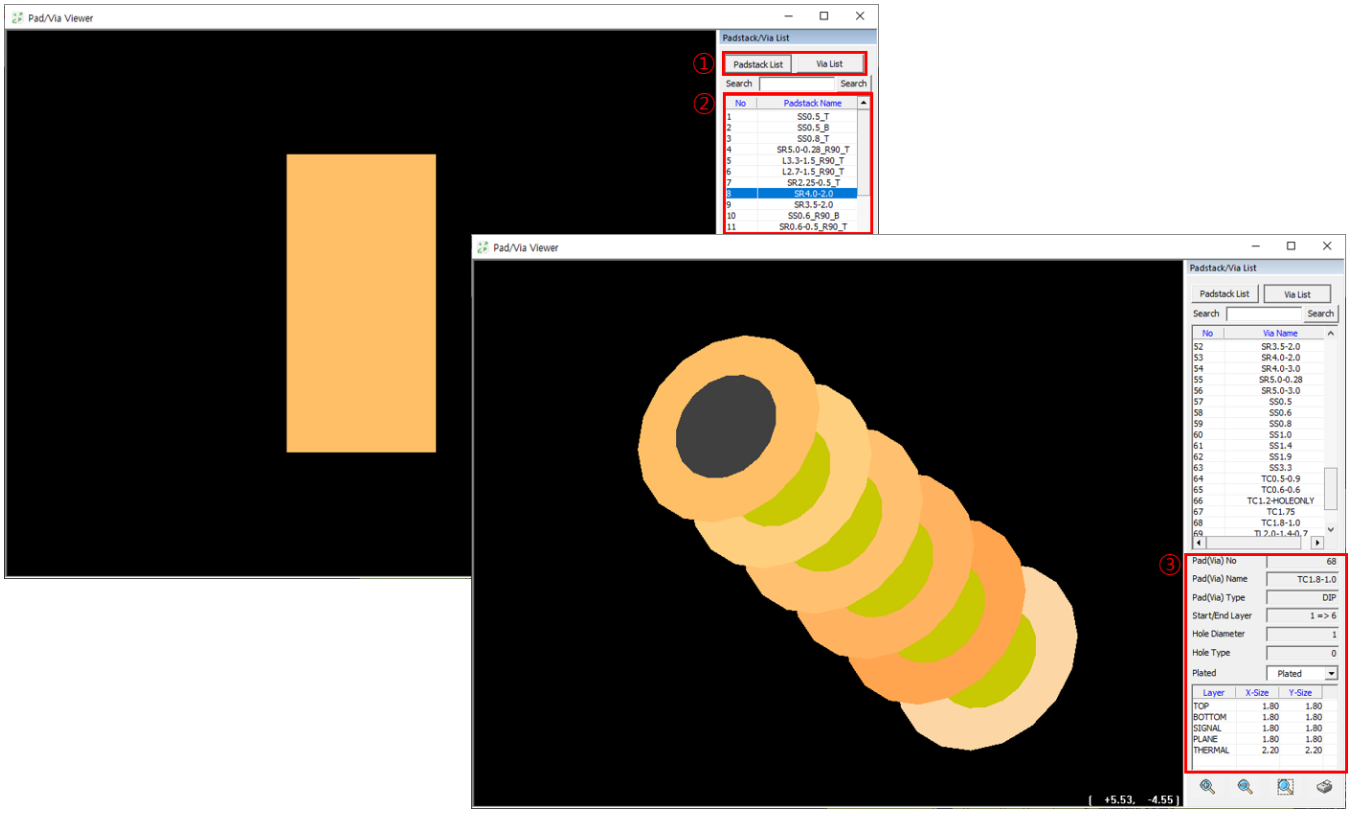
⑪ Using **Net 2D/3D Viewer** in **PCB Explorer**.



Upon launching “PCB Explorer”, at component list window, select component.
And use the menu, **Option > Net 2D/3D Viewer.** User can see the launched viewer for selected net.

4. **Padstack/Via Viewer**

Padstack/Via Viewer is viewer for reviewing padstacks or vias used in parts on active design. Use the menu, **Option > Padstack/Via Viewer**.

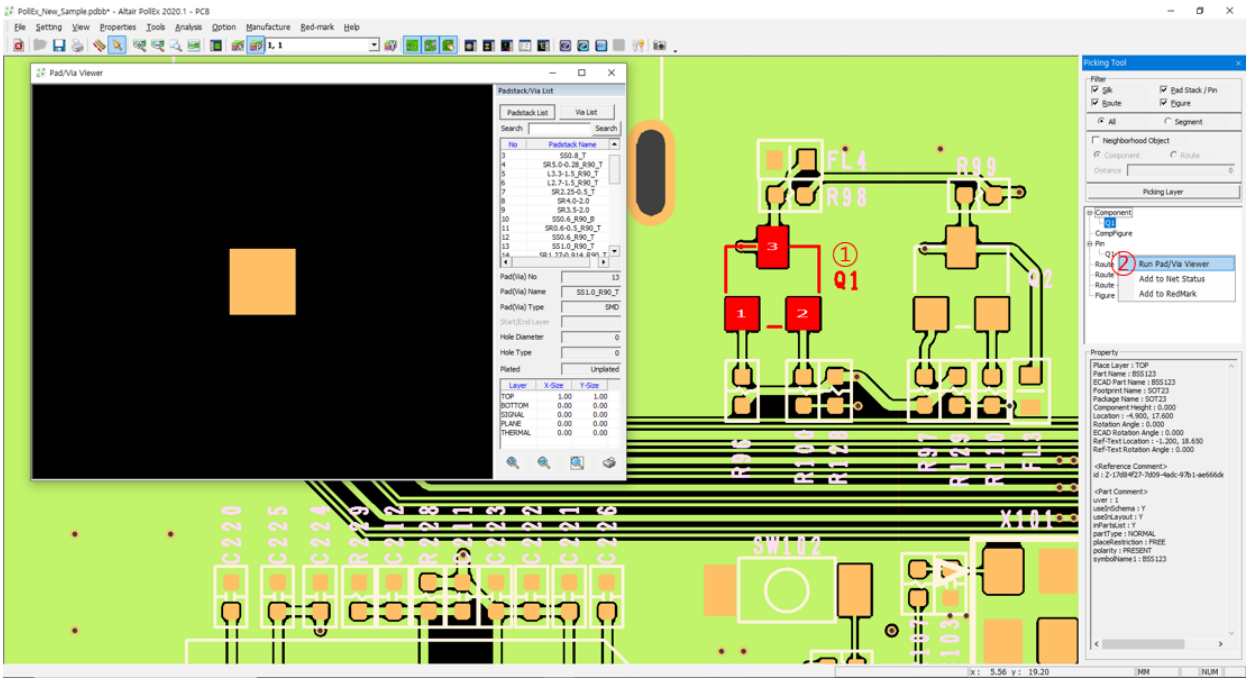


① Viewer mode selection for padstack or via.

② List for padstack or via depending on viewer mode. Upon selecting item in list, viewer will show it shape in 2D or 3D mode. Using 3D mode, user can check each physical layer's pad shape.

③ At information tab, there is much detail information for padstack or vias.

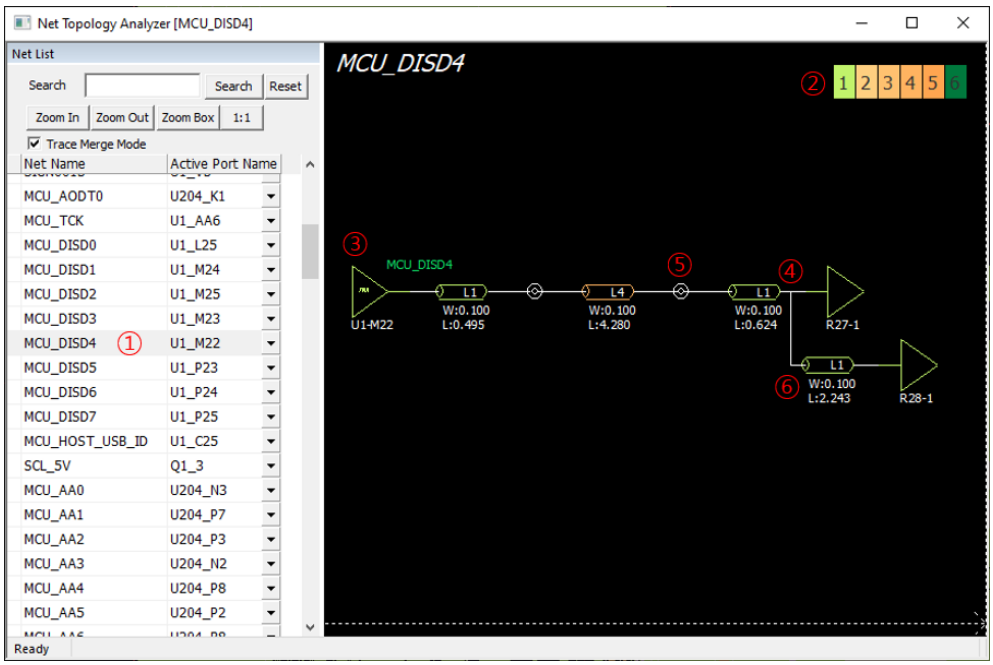
4.1. Using Padstack/Via Viewer in Picking Tool.



① Select objects using picking tool and at picking tool's list, select pin.
② Upon using mouse right button, select menu, **Run Pad/Via Viewer** among menu list.

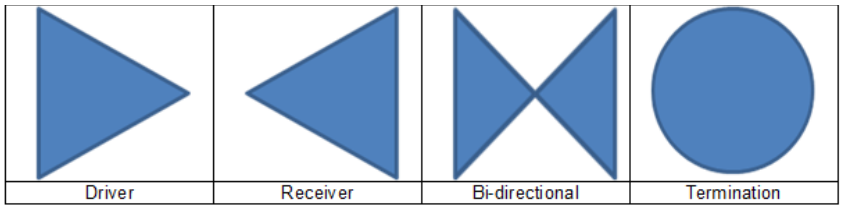
5. Net Topology Viewer

Net Topology Viewer is net viewer with showing topology style. From the base component pin, to the end connecting elements, this viewer shows all structures and composing elements' information(layer, pattern width, vias…). Use the menu, **Option > Net Topology Viewer**.



① Select the target net in the lists.
② Color table shows color of each physical layer. Elements on certain physical layers will be displayed as same color.

③ Base element should be the component's pin. Depending on pin's buffer types, shapes will be different.



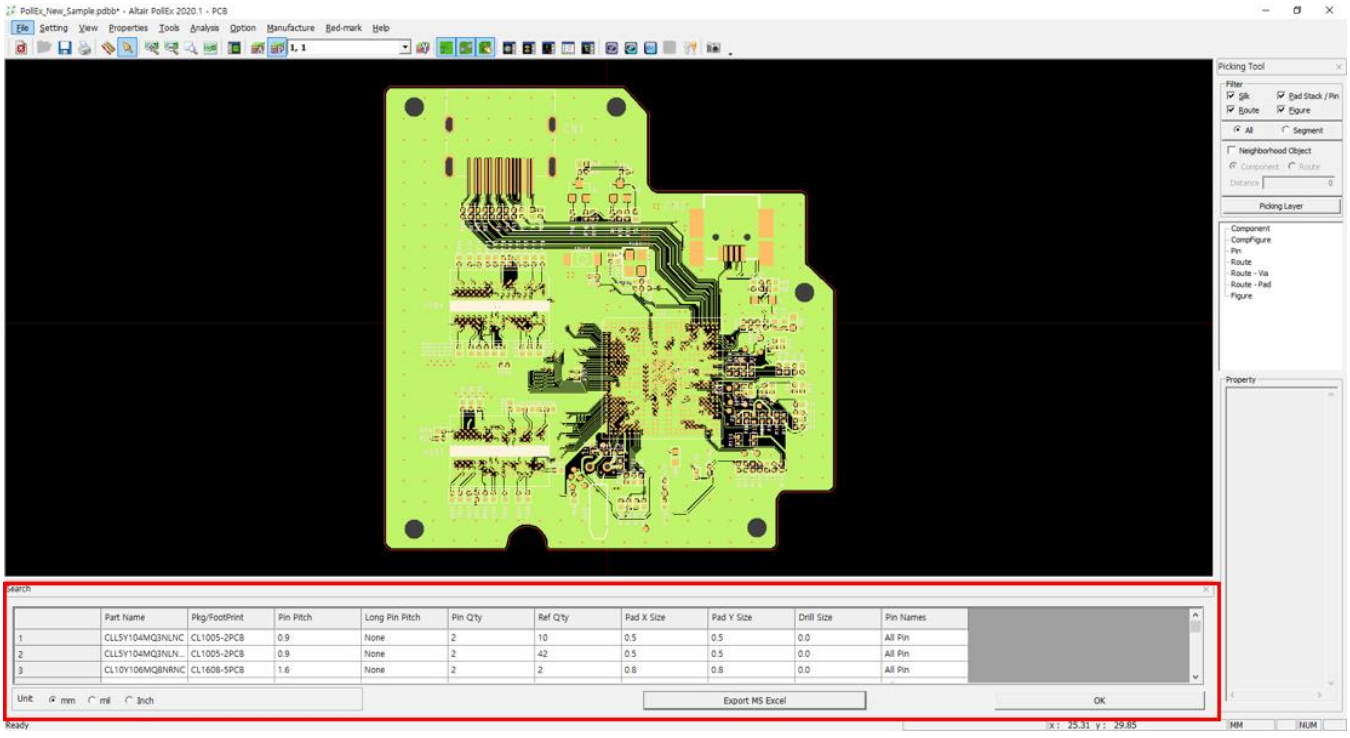
④ Branching node points.
⑤ Via symbol.
⑥ Routing pattern symbol. It may have information, layer with colors, length and width.

6. **Attribute Finder**

Make property list for components and their pins. Use the menu, **Option > Attribute Finder**.

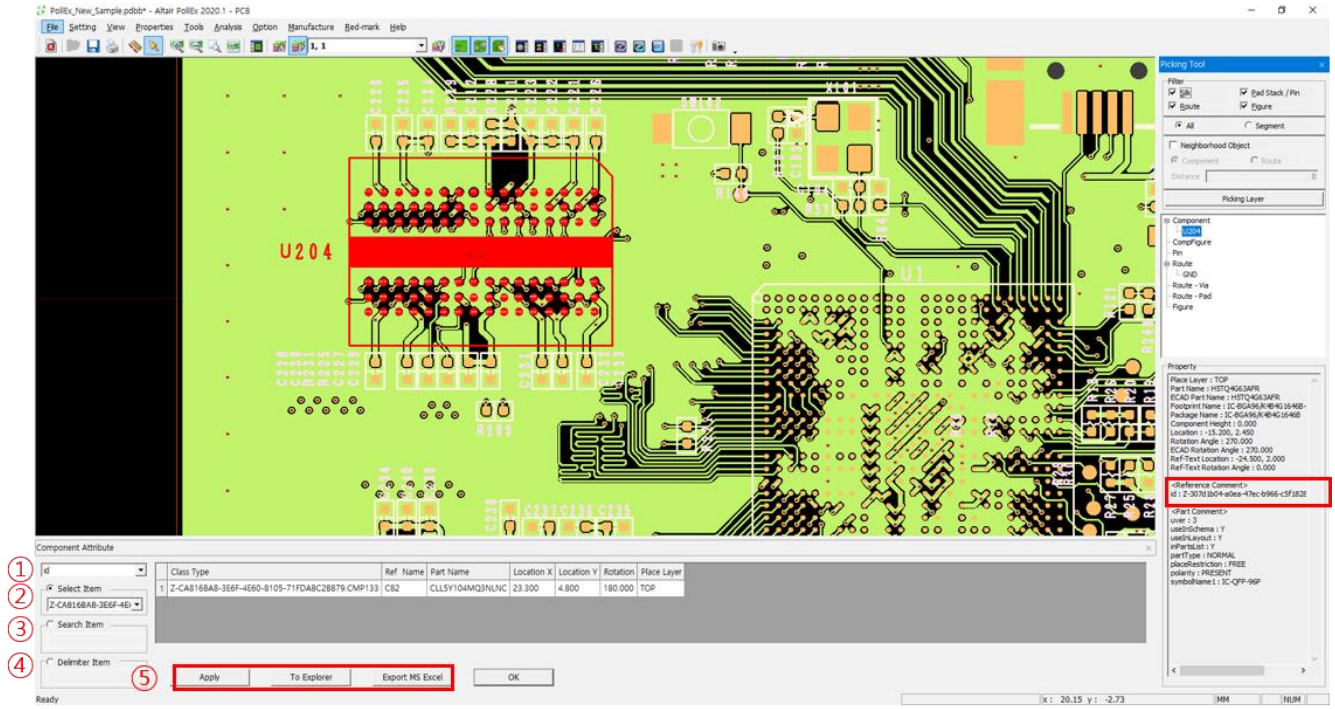
6.1. Search Parts Using Pin Pitches

This is searching parts using pin pitches. show pin pitch, pin or reference quantity etc. Also, user can export to excel contents. Click the list, then reference which is matched with selected part name will be highlighted.



6.2. Component Attribute

This function is used to find the references matched with selected reference property.



① All of reference property header listed. When you click **Apply** button, the reference name which is matched with selected property header is listed to right list box. If the selected Item is **All list**, all reference property will be displayed.

② All value of selected header in ① listed. If you select one of list and click **Apply** button, the reference name which is matched with selected property header and value is listed to right list box

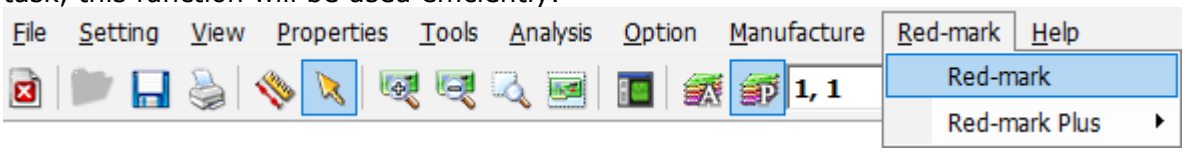
③ Enter the value of selected property header in ① to find. And click **Apply** button, the reference name which is matched with selected property header and value is listed to right list box

④ Enter the delimiter to separate the value based on input string.

⑤ Apply and to explorer or export to excel.

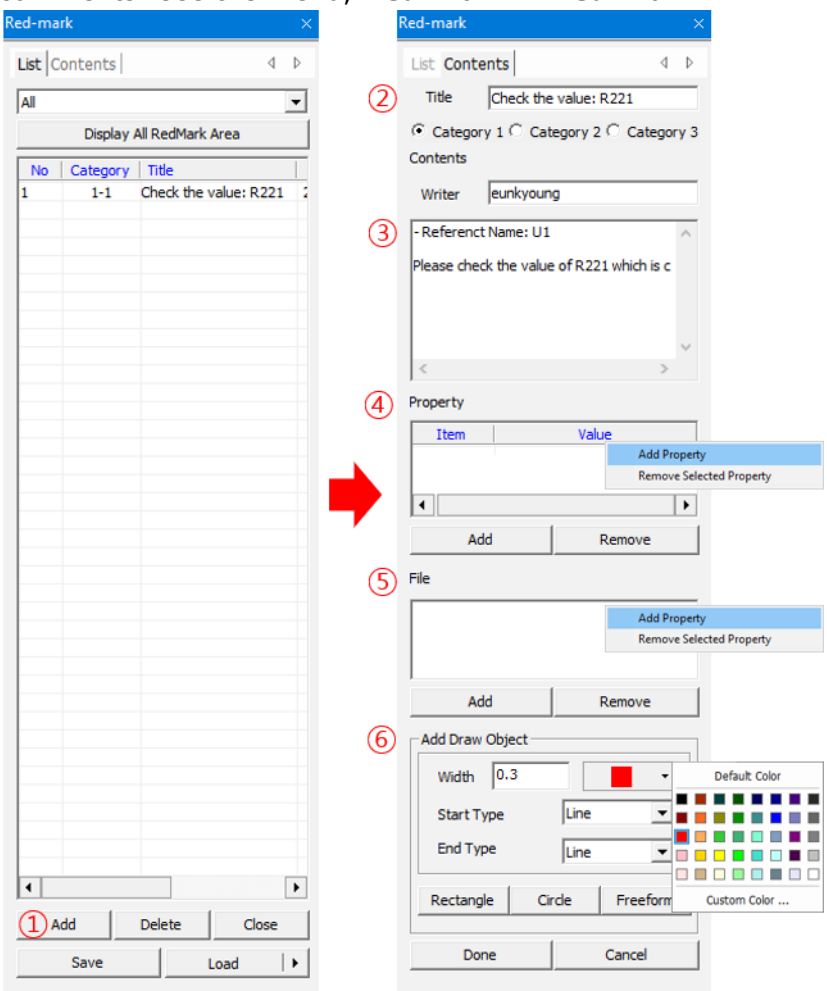
Red-mark

Red-Mark is a function to make comment on design. To leave message or comments for purpose to send task, this function will be used efficiently.

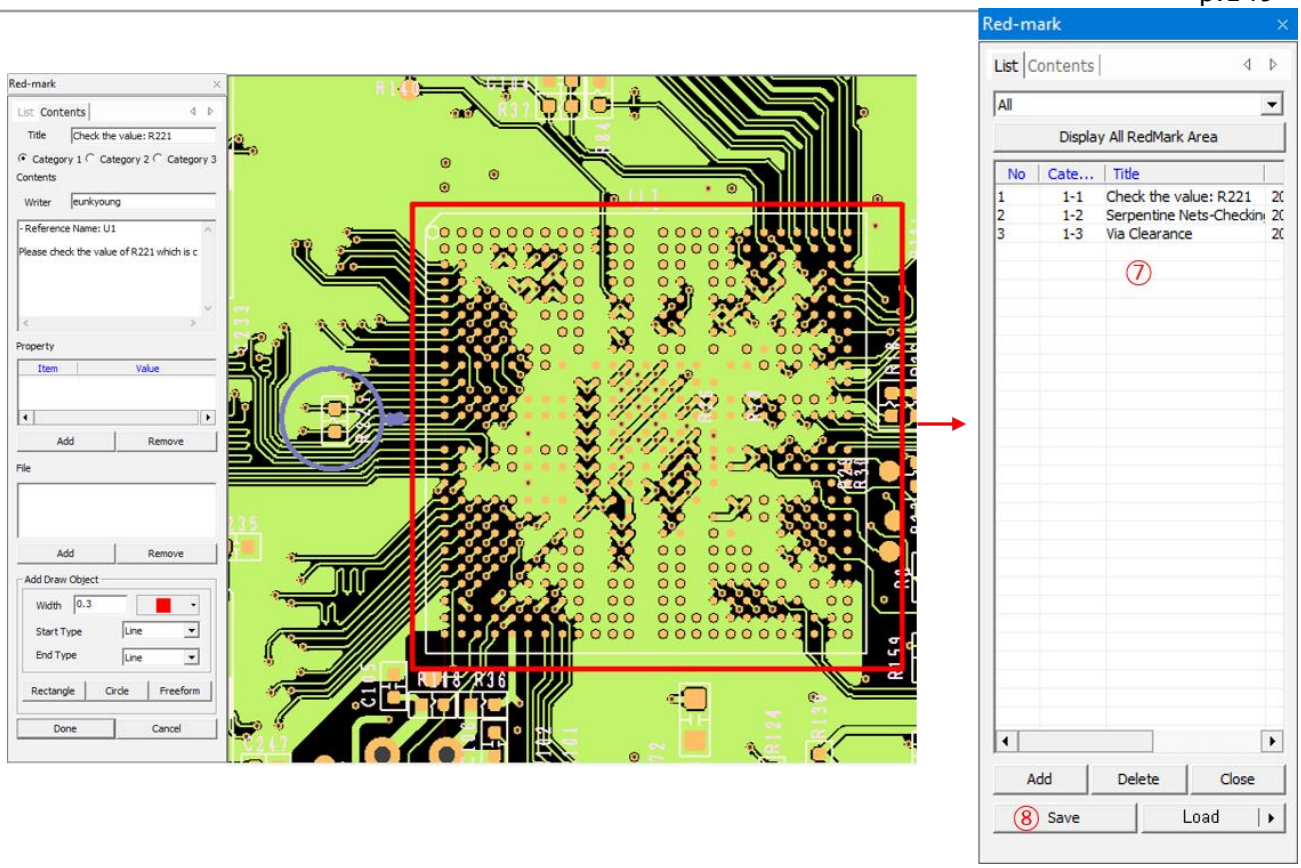


1. **Red-mark**

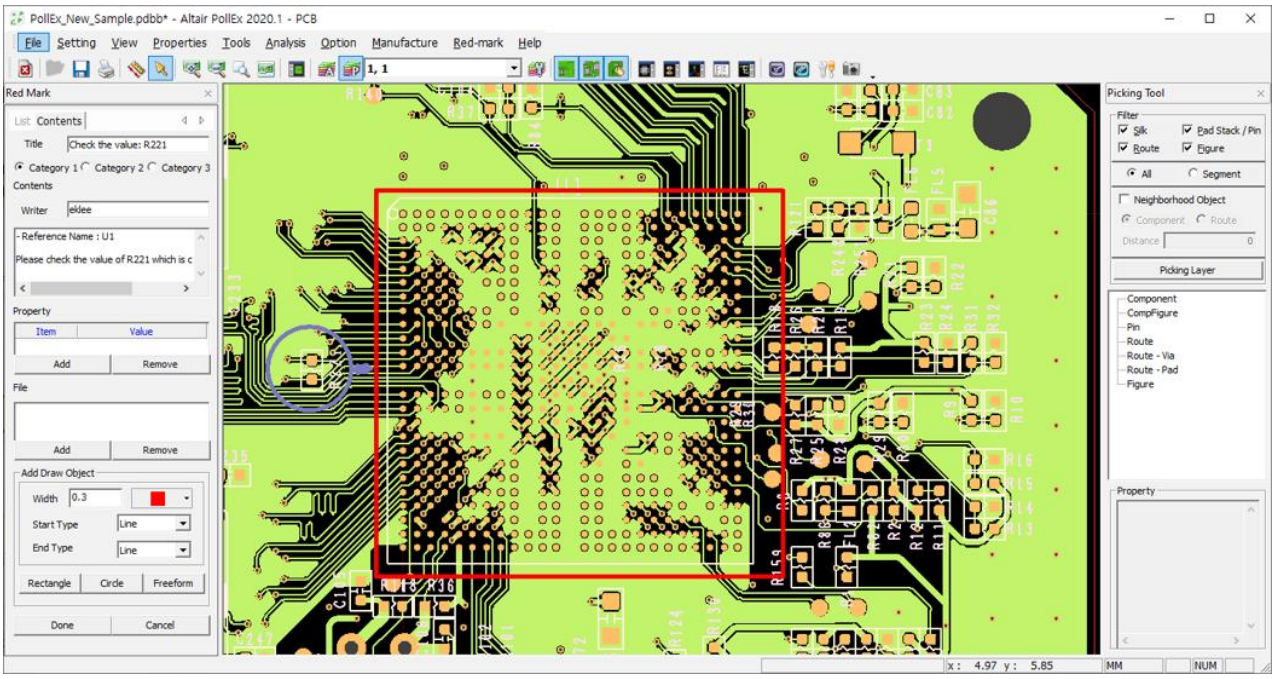
During exploring PCB design, if user input red-mark comment and save, all red-marks will be saved into PDBB file. So later, when other engineer open the design file, it is possible to see added red-mark comments. Use the menu, **Red-mark > Red-mark**.



① Use **Add**, **Del** or **Close** button to add, delete or close red-mark in list, respectively.
② Input new red-mark name.
③ Add message at this editing tab.
④ Add properties.
⑤ Attach file to Red-mark.
⑥ Select drawing object to make geometry into Red-mark. Supporting geometries would be circle, rectangle or arrow. Using geometries supported by **Red-mark**, user can express more easy and intuitive representation.



⑦ After adding Red-mark, user can see list of completed Red-marks.
⑧ Saving PDBB file in PollEx PCB will also save added red-marks into PDBB file.



※ When other users open the design, if there are red-marks are attached, PollEx PCB will open them automatically as upper picture.

2. **Red-mark Plus**
In Red-mark Plus, it is enabled to get the upgrade features for mark-up tools such as drawing object, text, measurement and reply, history etc.
Refer to the **Red-mark Plus** manual for detail instructions.