

Altair PollEx 2021

PCB User Guide

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Location	Telephone	E-mail	
Australia	+61 649 413 7981 anzsupport@altair.com		
Brazil	zil +55 113 884 0414 br_support@altair.com		
Canada	+1 416 447 6463	support@altairengineering.ca	
China	+86 400 619 6186	support@altair.com.cn	
France	+33 141 33 0992	francesupport@altair.com	
Germany	ny +49 703 162 0822 hwsupport@altair.de		
Greece	+30 231 047 3311	eesupport@altair.com	

Altair PollEx 2021 Technical Support

Location	Telephone	E-mail
India	+91 806 629 4500	support@india.altair.com
	+1 800 425 0234 (toll free)	
Israel		israelsupport@altair.com
Italy	+39 800 905 595	support@altairengineering.it
Japan	+81 36 225 5830	support@altairjp.co.jp
Malaysia	+60 32 742 7890	aseansupport@altair.com
Mexico	+52 555 658 6808	mx-support@altair.com
New Zealand	+64 9 413 7981	anzsupport@altair.com
South Africa	+27 21 831 1500	support@altair.co.za
South Korea	+82 704 050 9200	support@altair.co.kr
Spain	+34 910 810 080	support-spain@altair.com
Sweden	+46 46 460 2828	support@altair.se
United Kingdom	+44 192 646 8600	support@uk.altair.com
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12. Thermal Resistance Calculator	
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3. Radiated Emission	
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Conventions Used in this Guide

This guide uses the following conventions:

Bold All commands from the user interface. Options, menus, buttons, and dialog box names are bolded, but not italicized.

Example: On the **Welcome** screen, click **Next**.

Courier The path of a program or folder; a web address; a file name or component; text that the user is expected to enter.

Example: The default path is C:\Program Files\Altair\2020\PollEx

Questions regarding the document may be directed to PollEx team at PollEx support kr@altair.com.



PollEx Introduction

PollEx suite is knowledge-based design-verification toolset for PCB. It provides functions for all processes from concept design – schematic design – layout – verification(validation) – manufacturing to make them is most effectively used. In addition, it provides well customized environments which are widely used among various types of electronic process engineers. PollEx collects all functions which are used by design tools, manufacturing tools and process management solutions. With easy-to-use operation and versatile functions will guide users to the new electronic exploring.

1. PollEx PCB Concept

PollEx PCB can read ASCII files come from various types of ECADs or binary file having extension, PDBB. ASCII files from ECAD vendors are all different depending on ECAD suppliers. Users should know about the type of ECAD and their file extension before reading them into PollEx PCB program.

ECAD Vendors	Products	File Extension	Version
	PCAD	*.pcb	~PCAD 2006
Altium	Protel	*.pcb	%~Protel 99 SE
	Designer	*.PcbDoc	~16.0
	Allegro	*.comp, *.comppin, *.geom, *.lay, *.net, *.pad	all
Cadence	APD	After changing *.mcm to *.brd, use Allegro reading method.	all
	Spectra	*.dsn	all
	OrCAD Layout	*.dsn	all
CADVANCE		*.dsn, *.dbg, *.dbr	all
Autodesk EAGLE		*.brd	all
	BoardStation	*.geom, *.nets, *.comp, *.traces	all
Mentor	BoardStation (Neutral)	*.neutral, *.geom, *.trace	all
Graphics	Xpedition	Cell.hkp, JobPrefs.hkp, Layout.hkp, NetProps.hkp	all
	PADS	*.asc	5.0~
(Valor)	ODB++	Folder	all
ZUKEN	CADSTAR	*.cpa	all

Below table shows PollEx PCB supporting ECAD vendors and their ASCII files.



	CR5000 - Board Designer	<pre>Single board: *.pcf, *.ftf Arrayed board: *.pnf, *.ftf</pre>	7.0
	CR5000 - PWS	*.bsf, *.ccf, *.mdf, *.udf, *.wdf	all
IPC2581B		*.xml	all
CAM350		*.cam	all
Carbar	RS-274D	-	all
Gerber	RS-274X	-	all
	PollEx PCB (Binary)	*.PDBB	3.0~
PollEx	PollEx PCB (ASCII)	*.pdba	4.0~
	PollEx PCB	*.pdbx	2020

*The extension of Altium Protel 99 SE is same with *.pcb, but the format is the same as Altium Designer.
So, user should import ASCII file with using 'Altium Designer' menu.

If user has other formats which are not supported by PollEx PCB, users can be supported by UCS(User Customizing Service).

2. PollEx PCB Launching

Launch the menu, Start\Altair\2020\PollEx\PollEx_Launcher.exe.

Launch from the directory, C:\Program Files\Altair\2020\PollEx\PollEx_Launcher.exe.

3. PollEx PCB Windows

Below picture is the launched PollEx PCB main window.







Ready (5)

- ① Users can review the layout design at here, main window viewing area.
- 2 At the top of main frame window, user can see the version of PollEx PCB and active file name and path.
- ③ Menu Bar gives users many useful functions.
- ④ Tool-Bar menu gives users easy and institute icon menu.
- 5 Status-Bar menu shows current application status.
- 6 PollEx PCB shows the location of mouse cursor point.
- ⑦ Show the unit of active PCB layout design.
- 8 Picking-Tool box show the information of mouse-selected objects.

4. PollEx Menu Structure

PollEx PCB has 8 menus in menu bar. They will guide user to easily explore PCB layout.

Menu	1enu Sub-menu S		Description	
	Import ECAD		Read various types of ECAD.	
	Export to		PDB ASCII(*.pdba), PDB XML(*.pdbx), EDA Vender's Format, Restricted PDBB, DXF, GDSII	
	Open PDB Binary File	Ctrl+O	Open saved PollEx PCB file.	
	Save	Ctrl+S	Save into PollEx PCB file.	
File	Save As		Save as different name PollEx PCB file.	
	Save As Project		Create project folder for data handling in case of SI/Thermal analysis.	
	Print	Ctrl+P	Print into paper or Bitmap/Postscript image.	
	Close		Close active working.	
	Recent PDBB File List		List out and read recently imported file.	
	Exit		Exit from PollEx PCB.	
Satting	Environment		Set default PollEx PCB using environments.	
Setting	Layer	Alt+L	Set/View PollEx PCB's layer status.	



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		Measure		Measure the distance between objects.		
		Picking		Check the properties of objects.		
		Unit Conversion		Change the unit of PCB layout.		
		Board Information		See the whole board information.		
		Previous		Go back to previous viewing status(under construction).		
		Next		Go to next viewing status(under construction).		
		Zoom In	+, wheel↓	Zoom in viewing status.		
		Zoom Out	-, wheel ↑	Zoom out viewing status.		
		Zoom Window	Alt+W	Zoom in for mouse two picking points.		
		Zoom 1:1	Alt+1	PollEx PCB default design viewing status.		
		Toggle 1:1	Ctrl +Tab	Go to default window and shows previous Zoom in area.		
		Set Capture Window	Mouse Click & Ctrl+C	Save mouse clicked area into system buffer.		
	View	Mirror View	Ctrl+M	Shows mirrored PCB image.		
		Board Rotation		Rotate PCB for given rotation angle.		
		Route On/Off		Toggle for displaying routing pattern On/Off.		
		Component On/Off		Toggle for displaying component On/Off		
		Polygon Fill		Toggle for displaying polygon Fill/UnFill		
		Display Setup		Set status for displaying route/via/component.		
		Net Display On/Off		Toggle for displaying net On/Off.		
		Board Mini-Map		Show current viewing area regarding to whole PCB layout area.		
		Menu Bar		Toggle for showing menu-bar On/Off.		
		Tool Bar		Toggle for showing toolbar On/Off.		
		Status Bar		Toggle for showing status-bar On/Off.		
		Nets		Show netlist and nets' properties.		
		Composite-nets		Show all composite nets' properties.		
		Net Classes		Show all net classes		
		Net Buses/Group		Show all Buses/Group		
	Properties	Parts		Show partlist and linkage status with local part library.		
		Components		Show component list and assign passive component type.		
		Material Library		Show materials' properties.		
		Layer Stack		Show/Edit PCB layout Stack-Up.		
		Rigid-Flexible PCB		Define the flexible PCB area		
		Find /Query	Alt+Q	Find or query for component and net.		
		PCB Explorer	Ctrl+F	Explore components, nets or combinations.		
		Change Reference Names		Change reference names.		
	Tools	Change Board Origin		Change the origin point of PCB design.		
		Go to Location	Alt+G	Move cursor point to the given location.		
		Component Arrangement Plan		Show the components' placement status.		
		PCB Data Extractor		Make document regarding components or		



РСВ

			nets.		
	Extact Decap Data		Make list for decoupling capacitors on PCB.		
	Net Color		Change/Save colors of routing nets.		
	Net Length View		Make list for all nets' length.		
	Net Analyzer		Make analyzing report for all nets on PCB.		
	Change Net Name		Change net name with using ruf file.		
	Thermal Resistance Calculator		Calculate thermal resistance.		
	Gerber Transformation		After reading Gerber file, change the origin of Gerber layers to fit with PCB design.		
	Visual Layer Composition		Make user specific layers' composition.		
	BOM Changer		Change ECAD Part Name based on BOM data.		
	Worksheet Planner		Launch Worksheet Planner tool.		
	Golden Sample		Launch Golden Sample tool.		
	Signal Integrity		Launch Signal Integrity analysis tool.		
Analysis	Power Integrity		Launch Power Integrity analysis tool.		
Allalysis	Radiated Emission		Launch Radiated Emission analysis tool.		
	Thermal		Launch board level thermal analysis tool.		
	Part Viewer		Parts viewer for all parts used in PCB design.		
	Real PCB Assembly Viewer		3D assembled PCB viewer using 3D package link. Also provide the exporting to STEP.		
	Net 2D/3D Viewer		Show routing nets' structure with 2D/3D.		
	Padstack/Via Viewer		Padstack/Via viewer for all used in PCB design.		
Ontion	Net Topology Viewer		Show net structure as topology style.		
Ορτισπ	DFM		Design For Manufacturing		
	DFE		Design For Electronics		
	DFE+		Design For Electronics Plus		
	DFA		Design For Assembly		
	DFx Core Running		Define the DFx input files		
	Attribute Finder		Make property list for components and their pins.		
Rod-mark	Red-mark		Feature to make comment on PCB design.		
	Red-mark Plus		Advanced feature of PCB design mark-up		
Help	HelpPollEx ManualF1Open PollEx PCB manual.		Open PollEx PCB manual.		



5. PollEx PCB Tool Bar

PollEx PCB provides toolbar for frequently used menus.



- ① File management functions
 - Close: Close active design.
 - Open: Open PDBB file.
 - Save: Save active design into PDBB file.
 - Print: Print current view status into paper or Bitmap/Postscript image.
- ② Measure/Picking tools
 - Provide the function to measure objects or find the properties of objects. Two dialog menus run as toggle mode.
 - Picking tool: For mouse selected objects, show all related properties on picking dialog box.
 - Measure tool: Measure objects' size or distance between various objects.
- ③ View control menu
 - Zoom In/Zoom Out
 - Window Zoom: Zoom area for mouse selected two points.
 - Zoom 1:1: Go back to default view status.
- ④ PCB Explorer
 - Using PCB Explorer, user can search components or nets and component/net composition.
- 5 Layer Control
 - Artwork Layer: View layers with artwork layer order.
 - Physical Layer: View layers with physical layer order.
 - Layer: For selecting layers, user can change layer viewing status or layer properties.
- 6 Object Display On/Off Control.
 - Routing Data On/Off: Display On/Off function for route pattern.
 - Components Data On/Off: Display On/Off function for components on PCB.
 - Polygon Fill/Unfill: Display polygon or copper fill/unfill function.
- ⑦ Object Viewers/ Data Extraction Tool.
 - Parts Viewer: See all parts used in PCB layout.
 - Padstack/Via Viewer: See all padstacks and vias used in PCB layout.
 - Net 2D/3D Viewer: See all routing nets on PCB layout.
 - PCB Data Extractor: Documentation tool for nets or components and their related properties and objects. After making table, user can extract table information into MS/Excel sheets.
 - Net Topology Viewer: Show net routing structure with topology style.
- ⑧ DFM Core Running
 - Using this function, user can run PollEx DFM checking after specifying multiple DFM input files.
- 9 DFE Core Running



- Using this function, user can run PollEx DFE checking after specifying multiple DFE input files.
- 10 Metal Mask Manager
 - Using this function, user can checks whether a PCB design uses a standard metal mask.
- 1) Board Information
 - Window menu provide all information of working PCB. At dialog window, user can see file path, file generation date, board size, number of used component and nets... etc.
- 12 Capture
 - Using this menu, for selecting region with two points mouse picking and shortcut key, **Ctrl+C**, user can easily get image file on PCB.

6. Mouse Control

To efficiently operate, PollEx PCB provides some useful mouse operations.

1) Window zoom control: Zoom In/Out, mouse wheel up/down.

2) Panning: Window scroll, mouse right button click + Move.

3) Picking: use mouse left button. And if picking tool is active status, all selected objects' information will be shown on picking tool.

File

Here, user can check basic functions, importing ECAD files into PollEx PCB and exporting working design to 3rd party EDA vendors' format.

	, ,					
Eile	<u>S</u> etting	View	Properties	<u>T</u> ools	<u>A</u> nalysis	<u>O</u> pt
3	Import E	CAD				•
4	Export To)				►
	Open				Ctrl + C)
	Save				Ctrl + S	5
1	Save <u>A</u> s					
\smile	Save As P	roject				
	Save Proj	ect data	a into Compr	essed File	e (*.tgz)	
2	Print (5	\mathbf{D}			Ctrl + F)
	<u>C</u> lose					
6	Recent D	esign Fil	e List			►
	Exit					

- ① File Open and Save
 - **Open:** Import PollEx PCB's binary file, *.PDBB.
 - Save / Save As: Save active design into *. PDBB or different name of PDBB file.
 - Save As Project: Create folder for data handling.
 - Save Project data into Compressed File (*.tgz): Save the all of the current project data directory as a compressed file.
- ② File Close and Program Exit
 - Close: Close working job file.
 - Exit: Close PollEx PCB program.
- ③ Import ECAD
 - Import design from ASCII file which are created by other EDA vendors' CAD tools. PollEx PCB supports various types of prominent ECAD vendors' format.
- ④ Export To
 - **PDB ASCII** (*.pdba): User can save and export the design file with the ASCII format.
 - **Restricted PDBB**: User can save and export the design file with the user defined information.
- 5 Print
 - PollEx PCB can print active window image into printer or images like bitmap or postscript style.
- 6 Recent PDBB File List
 - import design from recently opened lists.

1. File Open / Save

PollEx PCB's binary data file has PDBB extension. After reading ASCII file from ECADs using PollEx PCB, user can save or import these files into PollEx PCB.

- Using the menu, **File > Open** with PDB Binary File (Shortcut key: **Ctrl + O**).



- Using the menu, Recent PDBB File List

Upon selecting design from recently used PDBB file list, user can easily open file. If user did not save design file or unstably closed case, the design file is not stored into the recent file list.

- Save / Save As



p.20

Use this menu to save current design to PDBB file. The one of merits of PDBB file is small file size compare to original ECAD design file. So, sending design to others or management will also be easy and fast without any loss of information.

Save current design using the menu, **File > Save/Save As** (Shortcut key: **Ctrl + S**).



2. File Close and Program Exit

User can use this menu to close active design or exit from PollEx PCB program.

Close active design using the menu, **File > Close**.

|--|--|

- Exit from PollEx PCB using the menu, **File > Exit**.

3. Import ECAD

All ECAD tools have their ASCII structures to be used by the 3rd party applications. PollEx PCB can import those ASCII files from various ECAD vendors. Depending on different types of ECAD ASCII files, this manual provides the way of importing them.

____Use the menu, File > Import ECAD > Select ECAD Tool to read ECAD's ASCII file.



- 1 ECAD vendor lists which PollEx PCB can import.
- ② CAM350, Gerber file importing menu. The purpose of GERBER file reading is to compare GERBER to PCB layout design. So, the number of readable GERBER layers have limitation in PollEx PCB. As the purpose of reviewing GERBER file, PollEx CAM is recommended.
- ③ ASCII, XML File importing menu, generated by PollEx PCB.
- User also can access the Import ECAD menu from Right-mouse click > Pop-up window> Select ECAD Tool.



3.1. Altium PCAD/Designer Interface PollEx PCB supports various Altium's PCAD, Protel and Designer files.

3.1.1. Altium PCAD

Step1. Extract PCAD ASCII file, *.pcb in Altium PCAD.

Step2. Use the menu, **File > Import ECAD > Altium PCAD**.

	Altium PCAD (*.pcb)
	Altium Designer (*.PcbDoc)
	Cadence - Allegro Expansion
	Cadence Specctra, Cadence OrCAD
	CADVANCE
	Autodesk EAGLE (*.brd)
	MentorGraphics - Board Station
	MentorGraphics - <u>N</u> eutral File
	MentorGraphics - Xpedition
	MentorGraphics - PADS (*.asc)
	ODB++
	Zuken - Cadstar(*.cpa)
	Zuken - CR5000 <u>B</u> oardDesigner
	Zuken - CR5000 PWS
	IPC-2581
	CAM350
	Gerber(RS-274D/RS-274X)
6	Open Ctrl + O
	Read PDB ASCII(*.pdba)
	Read PDB XML(*.pdbx)

Step3. At file selection dialog box, select the target ASCII file, *.pcb to import it.

🌮 Open				×
← → × ↑ 📙 « Te	mp > Altair-PollEx > PCB > Import	✓ Õ	earch Import	Ą
Organize 👻 New fold	er		833 -	• • •
Quick access OneDrive This PC Network	Name ^	Date modified 10/15/2018 1:01 PM	Type PCB File	Size 184 KJ
File <u>r</u>	۲ معرف معرف معرف معرف معرف معرف معرف معرف	į	All Files (*.pcb) Open	Cancel

There is a format to import Altium PCAD as below. [Example of *.pcb]



ACCEL_ASCII "F:\Temp\accel_demo.pcb"

```
(asciiHeader_
  (asciiVersion_2_2)
  (timeStamp_1998_6_4_9_35_21)
  (program_"ACCEL_P-CAD_PCB"_"13.00.38")
  (copyright "Copyright © _1997_ACCEL_Technologies,_Inc.")
  (fileAuthor_"T. Luong")
  (headerString_"License:_4172-3005_150738_Wolfgang_Schenke_Router_Solutions___")
  (fileUnits_Mil)
)
(library_"Library_1"
  (padStyleDef_"(Default)"
  (holeDiam_38.0)
  (StartRange_1)
   (EndRange_2)
   (padShape(layerNumRef_1) (padShapeType_Ellipse)_(shapeWidth_60.0)_(shapeHeight_60.0)_)
   (padShape_(layerNumRef_2)_(padShapeType_Ellipse)_(shapeWidth_60.0)_(shapeHeight_60.0)_)
```

3.1.2. Altium Designer

Step1. Extract Altium Designer ASCII file, *.PcbDoc in Altium Designer. Step2. Use the menu, **File > Import ECAD > Altium Designer**.

	Altium PCAD (*.pcb)	
	Altium Designer (*.PcbDoc)	
	Cadence - Allegro Expansion	
	Cadence Specctra, Cadence OrCAD	Import from Altium Designer X
	CADVANCE	
	Autodesk EAGLE (*.brd)	Layer Set-Up
	MentorGraphics - Board Station	COC (Place Boundary) Top Default
	MentorGraphics - <u>N</u> eutral File	COC (Place Roundary) Rottom Default
	MentorGraphics - Xpedition	COC (Place Boundary) Boctonn
	MentorGraphics - PADS (*.asc)	Board Outline Default
	ODB++	Use 0 for COC line width
	Zuken - Cadstar(*.cpa)	
	Zuken - CR5000 <u>B</u> oardDesigner	Apply to Environment Setting
	Zuken - CR5000 PWS	Designer ASCII File (*.PcbDoc)
	IPC-2581	Import Cancel
	CAM350	
	Gerber(RS-2/4D/RS-2/4X)	Reading and Converting Status
\geq	Open Ctrl + O	
	Read PDB ASCII(*.pdba)	
	Read PDB XML(*.pdbx)	

Step3. At file selection dialog box, select the target ASCII file, *.PcbDoc to import it.

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20 Open				×
← → × ↑ 📙 « Temp	p > Altair-PollEx > PCB > Import	v 0	Search Import	Q
Organize 👻 New folder				• •
Quick access CneDrive This PC Network	Name ^	Date modified 10/15/2018 1:01 PM	Type PCBDOC File	Size
<				3
File <u>n</u> an	ne:	~	All Files (*.PcbDoc) Open	∼ Cancel

There is a format to import Altium Designer as below.

*The extension of Altium Protel 99 SE is same with *.pcb, but the format is same as Altium Designer. So, user has to import ASCII file with using 'Altium Designer' menu.

3.2. Cadence Allegro Expansion/Spectra/OrCAD Interface

Cadence does not support ASCII extraction menu itself, but users can use executable file, extracta.exe to get ASCII files. To use this command, users do not need license but Allegro installation environment.

- 3.2.1. Cadence Allegro Expansion
- 1) Direct Allegro file reading using binary file, *.brd.
- 2) Allegro file reading using ASCII files.

3.2.1.1. Direct Allegro file reading using binary file, *.brd.

Step1. Setup Environment for Interface

Once user sets environment for Allegro, every time when users import Allegro file in PollEx PCB, user does not need any other additional setting.



🕫 Environment		×
General View Layer Layer Status Layer Stack	Cadence - Allegro Expansion Encoding Convert EUC-JP to Shift JIS	
Picking Picking Picking	Import Type C Allegro Binary File Allegro ASC Binary Reading Option	II Files C Allegro Fabmaster File
Altium PCAD Altium Designer <mark>Cadence - Allegro Expansion</mark>	3)Path to the extracta.exe Path to the Control File Options	C:₩
MentorGraphics - Board Station, Neutra MentorGraphics - Xpedition MentorGraphics - PADS (*.asc) ODB++ Zuken - CR5000 Board Designer	Allow Broken Component Allow Broken Component Higher than Version 16.3 Add suffix "Manufacturing" for the manuf Laver Set In	facturing related layers
Zuken - CR5000 PWS	Path to the layer set-up file	C:₩ []
Analysis	COC (Place Boundary) Top	PLACE_BOUND_TOP
Metal Mask Manager	COC (Place Boundary) Bottom	PLACE_BOUND_BOTTOM
Block Design Generator	Silk Top	SILKSCREEN TOP
- DFM	Silk Bottom	STLKSCREEN BOTTOM
DFE	Reard Outline	
··· DFE+	board Oddine	POR POR
	пое	HOLE
Component Mounting Emulator	Save layer	set-up data
Save Load		OK Cancel

- ① Select menu, Setting > Environment > ECAD > Cadence Allegro Expansion.
- $\ensuremath{\textcircled{}^\circ}$ Set the default reading type whether user import design from binary or ASCII file.
- ③ If user wants to use the way of reading binary file, set executable command file, extracta.exe path. Example: %ALLEGRO INSTALL DIR%\tools\pcb\bin
- ④ To use Allegro ASCII extraction command, extracta.exe, user need to use control file for extract ASCII file. Set the path for control file. Example: C:\Users\%USER NAME%\AppData\Roaming\Altair\PollEx\Share\AllegroExpans

C:\USErs\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share\AllegroExpans ion_ExtractCommandFile163.txt

- ⑤ Check whether user wants to use break component or not. Break Component means reference components which are different than prototype in library.
- 6 Check **Higher than Version 16.3** when user wants to read the design from Allegro version 16.3.



Step2. Allegro design reading using original binary file, *.brd – use one of following two ways.

File > Import ECAD > Cadence - Allegro Expansion

Altium PCAD (*.pcb)					
Altium Designer (*.PcbDoc)					
Cadence - <u>A</u> llegro Expansion					
Cadence Specctra, Cadence OrCAD					
CADVANCE					
Autodesk EAGLE (*.brd)					
MentorGraphics - Board Station					
MentorGraphics - <u>N</u> eutral File					
MentorGraphics - Xpedition					
MentorGraphics - PADS (*.asc)					
ODB++					
Zuken - Cadstar(*.cpa)					
Zuken - CR5000 <u>B</u> oardDesigner					
Zuken - CR5000 PWS					
IPC-2581					
CAM350					
Gerber(RS-274D/RS-274X)					
Read PDB XML(*.pdbx)					
				-	
Import from Cadence Allegro	>	×	User Defined Setting for Cadence A	llegro	×
Import from		1	C Allegro Binary File I A	llegro ASCII Files C	Allegro Fabmaster File
Design File (* brd * mcm)			- Binary Reading Ontion		
			Path to the extracta.exe	C:₩	
			2 Path to the Control File		
Allegro ASCII Files			Options		
Geom (*Geom.txt)			Allow Broken Component		
Panel			Higher than Version 16.3		
C Allegro Fabmaster File			Add suffix Manufacturing to	or the manufacturing related	layers
Fabmaster (*.txt, *.cad)			COC (Rhoo Roundany) Tan	PLACE BOUND TOP	
			COC (Place Boundary) Top COC (Place Boundary) Bottom	PLACE BOUND BOTTOM	
User Defined Setting			Silk Top	SILKSCREEN_TOP	
Import	Cancel	1	Silk Bottom	SILKSCREEN_BOTTOM	
]	Board Outline	BOARD_OUTLINE	
Reading and Converting Status			4 Hole	HOLE	
			Apply to Environment Setting	ОК	Cancel
		-			

Item ① are showing the contents set on environment. At ②, select the Allegro binary file, *.brd and press the button menu, **Read from Binary** will start reading Allegro file. If the check box ③ is ON status, PollEx PCB Allegro reader will check Allegro version whether it is version 16.3 or not.

Hole (4): For the design file created by Allegro version 16.3, if there is another defined hole on certain layer, specify the hole layer name.

Using the environment setup, user does not need to setup Allegro reading parameters at this window.

3.2.1.2. Cadence – Allegro Expansion



🌮 Open			×
← → ~ ↑ 📙 « Im	nport > Cadence Allegro Expansion	V Ö Search Ca	adence Allegro Expa 🔎
Organize 🔻 New fold	ler		🎫 🕶 🔲 💡
1 Oristanov	Name	Date modified	Туре
Quick access	test_Comp	3/25/2013 2:18 PM	Text Document
OneDrive	test_Geom	3/25/2013 2:18 PM	Text Document
This DC	test_Lay	3/25/2013 2:17 PM	Text Document
- msec	test_Net	3/25/2013 2:18 PM	Text Document
Network	i test_Pad	3/25/2013 2:17 PM	Text Document
	itestCompPin	3/25/2013 2:17 PM	Text Document
	<		,
File <u>n</u>	jame:	 Allegro [)ata File (*.txt; *Lay.txt;
		Ope	n Cancel
		-	

- As the same with Allegro reading case, Allegro Expansion reading also left some of ASCII files. In this case, there are 6 ASCII files, *.Comp, *.CompPin, *.Geom, *Lay, *.Net and *.Pad. PollEx PCB reads these 6 files after running extracta.exe command.
- 3.2.2. Allegro file reading using ASCII files.

Step1. Extracting ASCII File

Following two windows guide users to extract ASCII file from Allegro binary design file, *.brd.

3.2.2.1. Allegro Expansion Reading Case.

Use the Allegro ASCII file extraction command, AllegroExpansionASCIIExtractor.exe in the path, C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share.

Allegro Expansion Ascii File Extractor		
Allegro Expansion	C Allegro	
Allegro Extract Command (extracta.exe)	1	[]
Extract Command File (*.txt)	2	
Design File(*.brd)	3	
Extract ASCII Design File		

At ①, specify the Allegro ASCII extraction command file, extracta.exe path.

- At ②, give the control file, AllegroExpansion_ExtractCommandFile.txt path under C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share.
- At ③, select target Allegro design file.

Upon pressing the button, Extract ASCII Design File will make 6 different ASCII files.

Step2. Import Allegro using ASCII file.

Use one of following two menus to import Allegro design.

File > Import ECAD > Cadence - Allegro Expansion



Altium PCAD (*.pcb)	Import from Cadence Allegro
Altium Designer (*.PcbDoc)	- Impart from
Cadence - <u>A</u> llegro Expansion	
Cadence Specctra, Cadence OrCAD	
CADVANCE	
Autodesk EAGLE (*.brd)	Panel
MentorGraphics - Board Station	
MentorGraphics - Neutral File	
MentorGraphics - Xpedition	
MentorGraphics - PADS (*.asc)	Panel
ODB++	
Zuken - Cadstar(*.cpa)	C Allegro Fabmaster File
Zuken - CR5000 BoardDesigner	Fabmaster (*.txt, *.cad)
Zuken - CR5000 PWS	
IPC-2581	User Defined Setting
CAM350	Import Cancel
Gerber(RS-274D/RS-274X)	
🌽 Open Ctrl +	Reading and Converting Status
Read PDB ASCII(*.pdba)	
Read PDB XML(*.pdbx)	

At ①, to read Allegro design with ASCII file, the reading type check button should be **Read from ASCII File**. User can set this setting in environment.

Using the button ② for Allegro Expansion reading, users can select ASCII files. Finally, upon pressing the button, **Read from ASCII**, import selected ASCII files and convert them to PollEx PCB design job file, *.PDBB.

3.2.3. Cadence - Spectra/OrCAD

The file extension of Cadence Spectra is *.dsn. Schematic file of Cadence OrCAD has also same file extension, so be cautious when user selects file.

Step1. Extract ASCII file, *.dsn from Cadence Spectra. Step2. Use the menu, **File > Import ECAD > Cadence Spectra/Cadence OrCAD**.





Another way of reading Spectra file is using utility program of Allegro. Allegro utility program converts Spectra file to Allegro design file, *.brd and uses Allegro reader in PollEx PCB.

3.2.4. CADVANCE Interface PollEx PCB supports CADVANCE files such as *.dsn, *.dbg and *.dbr files.

Step1. Extract ASCII file, *.dsn,*.dbg,*.dbr from CADVANCE.Step2. Use the menu, File > Import ECAD > CADVANCE.

	Altium Designer (*.PcbDoc)	
	Cadence - <u>A</u> llegro Expansion	
	Cadence Specctra, Cadence OrCAD	
	CADVANCE	
	Autodesk EAGLE (*.brd)	Import from CADVANCE X
	MentorGraphics - Board Station	- Lawer Set Lin
	MentorGraphics - <u>N</u> eutral File	1 Board Outline
	MentorGraphics - Xpedition	Except Laver
	MentorGraphics - PADS (*.asc)	
	ODB++	Apply to Environment Setting
	Zuken - Cadstar(*.cpa)	Cadvance ASCII File
	Zuken - CR5000 <u>B</u> oardDesigner	DSN (*.dsn)
	Zuken - CR5000 PWS	DBG (*.dbg)
	IPC-2581	DBR (*.dbr)
	CAM350	
	Gerber(RS-274D/RS-274X)	Import Cancel
0	Open Ctrl + O	Reading and Converting Status
	Read PDB ASCII(*.pdba)	
	Read PDB XML(*.pdbx)	



- ① If there is a specific layer for board outline, specify the layer name. This layer will be transferred to layer number 21 in PDB structure.
- ② In case of CADVANCE Interface, it might be big data because it brings all layer's information from CADVANCE ASCII. So, it can be excepted the specific layer.

3.2.5. Autodesk EAGLE Interface

PollEx PCB supports EAGLE CAD file such as *.brd file.

Step1. Extract ASCII file, *.brd from Autodesk EAGLE.
Step2. Use the menu, File > Import ECAD > Autodesk.

	Altium PCAD (*.pcb) Altium Designer (*.PcbDoc) Cadence - <u>A</u> llegro Expansion Cadence Specctra, Cadence OrCAD	
	CADVANCE	
	Autodesk EAGLE (*.brd) MentorGraphics - Board Station MentorGraphics - Neutral File MentorGraphics - Xpedition MentorGraphics - PADS (*.asc) ODB++ Zuken - Cadstar(*.cpa)	Import from Autodesk EAGLE EAGLE ASCII File(*.brd) Import Cancel Reading and Converting Status
	Zuken - CR5000 <u>B</u> oardDesigner Zuken - CR5000 PWS IPC-2581 CAM350 Gerber(RS-274D/RS-274X)	
2	Open Ctrl + O Read PDB ASCII(*.pdba) Read PDB XML(*.pdbx)	

3.3. Mentor Graphics Interface

Mentor Graphics is releasing several different ECAD tools, PADS PowerPCB, Board Station and Expedition.

3.3.1. Mentor Graphics - Board Station

PollEx PCB's Mentor Graphics - Board Station reader use following 5 ASCII files.

File	Example		
comp.com_XXX	comps.comp_256		
net.net_XXX	nets.net_123		
traces.traces_XXX	traces.traces_123		
tech.tech_XXX	Tech.tech_123		
geometry file	*.geom		

In Board Station working folder, there are 4 files except Geometry file. Among many files, select a file having header, comp, net, and trace and tech files with the highest revision number. It means they are latest files. However, user does not need tech.tech_XXX file, if user did not use blind or buried via.

Step1. Extraction Geometry files in Board Station.



- 1. Open Job file and launch librarian.
- 2. Use the menu, **File > Save > Save ASCII Geometries**.
- 3. Select All Geometries and One File and save file in certain path with extension, *.geom.

Step2. Reading Mentor Graphics Board Station ASCII in PollEx PCB.

Use the menu, File > Import ECAD > Mentor Graphics - Board Station.

	Altium PCAD (*.pcb)	Import from MentorGraphics Board Station X
	Altium Designer (*.PcbDoc)	1-Layer Set-Up
	Cadence - Allegro Expansion	COC (Place Boundary) Top
	Cadence Specctra, Cadence OrCAD	
	CADVANCE	COC (Place Boundary) Bottom
	Autodesk EAGLE (*.brd)	Board Type
	MentorGraphics - Board Station	C Single Board C Array-Single Board C Array-Full Board
	MentorGraphics - <u>N</u> eutral File MentorGraphics - Xpedition MentorGraphics - PADS (*.asc) ODB++ Zuken - Cadstar(*.cpa) Zuken - CR5000 <u>B</u> oardDesigner Zuken - CR5000 PWS IPC-2581 CAM350 Gerber(RS-274D/RS-274X)	 Add Drawing Part to Reference Designator Exclude Silkscreen of 0 Line Width Include Hatched Copper Apply to Environment Setting Board Station ASCII Files ASCII Files Require 5 files (*tech, *comp, *net, *trace, *geom) Read Sub-Board Sub-Board ASCII File Directory
2	Open Ctrl + O Read PDB ASCII(*.pdba)	
	Read PDB XML(*.pdbx)	Import Cancel
		Reading and Converting Status

- ① Specify the artwork layer name to recognize as COC Top and Bottom.
- ② Select reading board type.
 - **Single Board**: Use this option for reading single board.
 - Array-Single Board: Use this option for reading array board contour and single board.
 - **Array-Full Board**: Use this option for reading array board contour and full single board.
- ③ Add drawing part to reference designator.
- ④ Exclude Silkscreen of 0 Line Width: Excludes silkscreen having a line width of zero.
- 5 Check this option if the hatched copper is used in the design.
- 6 At any column if user selects one among 5 ASCII files, others are automatically assigned to each folder column. At this time, if there are multiple files having same name but different version, PollEx PCB will automatically select the latest version.
- O Check this option when users use generic parts in array board and want them to be part of sub board.

3.3.2. Mentor Graphics - Neutral File

PollEx PCB also can read Board Station's neutral file and followings are necessary ASCII files for importing into PollEx PCB.

File Example



neutral_file	neutral.vss		
traces.traces_XXX	traces.traces_123		
tech.tech_XXX	tech.tech_123		
geometry file	*.geom		

If user did not use blind/buried via, tech.tech_XXX file is not needed.

Step1. Extract Geom file in Board Station

1. Open jog file and launch librarian.

2. Use the menu, **File > Save > Save ASCII Geometries**.

3. Select **All Geometries** and **One File.** Then, save file with extension name *.geom into a certain folder.

Step2. ASCII importing in PollEx PCB.

Use the menu, File > Import ECAD > Mentor Graphics - Neutral File.

Altium PCAD (*.pcb)	Import from MentorGraphics Neutral File	×
Altium Designer (*.PcbDoc) Cadence - <u>A</u> llegro Expansion	Mode Whole files Neutra	l Files
Cadence Specctra, Cadence OrCAD CADVANCE	2 Version © Board Station C Xpediti	on
Autodesk EAGLE (*.brd)	Apply to Environment Setting	
MentorGraphics - Neutral File	Neutral ASCII File (*.vss)	
MentorGraphics - Xpedition MentorGraphics - PADS (*.asc)	Geom ASCII File(*.geom)	
ODB++	Trace ASCII File(*.traces)	
Zuken - CR5000 BoardDesigner	Tech ASCII File(*.tech)	
Zuken - CR5000 PWS IPC-2581	Import	Cancel
CAM350 Gerber(RS-274D/RS-274X)	Reading and Converting Status	
Open Ctrl + O Read PDB ASCII(*.pdba)		

- Choose the type of ASCII file. Neutral Files will read only component placement and netlist information. There is no routing information. On the other hand, Whole Files will read all PCB related information. When selected Whole Files, PollEx PCB will read 4 files, tech.tech***, neutral, ASCII GEOM and trace.trace***.
- **2** Choose the version **Mentor Board Station** or **Mentor Xpedition**.
- ③ User can select necessary files individually.

Read PDB XML(*.pdbx)

3.3.3. Mentor Graphics - Xpedition

PollEx PCB read Mentor Graphics Xpedition's 6 ASCII files. Following table shows all necessary files and their information.

File Name	Description			
Cell.hkp	Component placement information			
JobPrefs.hkp	Layer information			
Layout.hkp	Routing information			
NetProps.hkp	Net information			
Padstack.hkp	Padstack information			
PDB.hkp	Part library information			

Step1. Extract ASCII file from Mentor Graphics Xpedition.

Step2. Use the menu, **File > Mentor Graphics – Xpedition**.

	Altium PCAD (*.pcb)						
	Altium Designer (*.PcbDoc)						
	Cadence - <u>A</u> llegro Expansion						
	Cadence Specctra, Cadence OrCAD						
	CADVANCE						
	Autodesk EAGLE (*.brd)						
	MentorGraphics - Board Station						
	MentorGraphics - <u>N</u> eutral File						
	MentorGraphics - Xpedition						
	MentorGraphics - PADS (*.asc)						
	ODB++						
	Zuken - Cadstar(*.cpa)						
	Zuken - CR5000 <u>B</u> oardDesigner						
	Zuken - CR5000 PWS						
	IPC-2581						
	CAM350						
	Gerber(RS-274D/RS-274X)						
6	Open Ctrl + O						
	Read PDB ASCII(*.pdba)						
	Read PDB XML(*.pdbx)						



After selecting all 6 files, pressing OK button will start reading Expedition into PollEx PCB.

Import from MentorGraphics Xpedition		>	<					
Layer Set-Up			1					
COC (Place Boundary) Top								
COC (Place Boundary) Bottom								
Board Outline	BOARD_OUTLINE							
Panel Outline	PANEL_OUTLINE							
Holo	Hole			🥻 Open				×
riole				← → ~ ↑ <mark> </mark> «	PCB > Import > Mentor Expedition	✓ Ö Search Ment	tor Expedition	P
Options			1	Organize 🔻 New f	older		EE 👻 🔲	?
ASCII File Directory	\$PCB₩Output₩Expo	ortDesignData		- Owiek access	Name	Date modified	Туре	
Hotel no brockery				A Quick access	Cell.hkp	9/24/2014 12:11 PM	HKP File	
Select Sub Board	M Read only One for	the Same Boards		len OneDrive	JobPrefs.hkp	9/24/2014 12:11 PM	HKP File	
				💻 This PC	Layout.hkp	9/24/2014 12:11 PM	HKP File	
Allow Broken Component	Allow Unconnected Net	Remove Net Data		- Naturali	NetProps.hkp	9/24/2014 12:11 PM	HKP File	
			i 🕞	- Network	DB bkp	9/24/2014 12:11 PM	HKP File	
Арр	ply to Environment Setting				PDB.nkp	5/24/2014 12:11 PW	FIRE FILE	
Xpedition ASCII Files (*.hkp)								
Require 5 files (JobPrefs, Cell, Padstaci	, k, Layout, PDB), Optional (N	letProps)	-					
Import		Cancel	1					
			1		<		_	>
Reading and Converting Status				5	h	Europhics (C
				FI	e name:	Expedition #	(SCII(JODPrefs.hkp;C	. ~
,			J			<u>O</u> pen	Cancel	

3.3.4. Mentor Graphics - PADS

Users can export Mentor Graphics PADS design to ASCII file, *.asc. Depending on ASCII version of PowerPCB, they might be different, but PollEx PCB will support every version of them.

Step1. Extract ASCII file from Mentor Graphics PADS.

Step2. Use the menu, **File > Import ECAD > Mentor Graphics – PADS**.

	Altium PCAD (*.pcb)		Import from MentorGraphics PADS X
	Altium Designer (*.PcbDoc)		Lawar Cat Un
	Cadence - Allegro Expansion		COC (Place Boundary) Top
	Cadence Specctra, Cadence OrCAD		
	CADVANCE		COC (Place Boundary) Bottom
	Autodesk EAGLE (*.brd)		Board Outline
	MentorGraphics - Board Station		Drill Dvor
	MentorGraphics - <u>N</u> eutral File		
	MentorGraphics - Xpedition	2	Solder Mask Top
	MentorGraphics - PADS (*.asc)		Solder Mask Bottom
	ODB++		
	Zuken - Cadstar(*.cpa)		
	Zuken - CR5000 <u>B</u> oardDesigner		Metal Mask Bottom
	Zuken - CR5000 PWS		Silk Top
	IPC-2581		
	CAM350		Silk Bottom
	Gerber(RS-274D/RS-274X)	0	Signal Layer in Part Section Signal Layer in Line Data Section
0	Open Ctrl + O		Level 0 is Board Outline Allow Broken Component
	Read PDB ASCII(*.pdba)		Options
	Read PDB XML(*.pdbx)	(4)	COC of 0 Line Width CAM Pad Over Size (Solder, Paste)
			Generate Teardrops Remove Duplicated Segments
			Apply to Environment Setting
			PADS ASCII File (*.asc)
			Import Cancel
			Reading and Converting Status



РСВ

- ① After selecting menu, **PADS ASCII File** (*.asc), press the button menu to read from PADS ASCII file.
 - ② **Layer Setting** is an optional. Specify artwork layer name per each menu.
 - COC Top/bottom: PollEx DFM will use these layers' data for measure base.
 - Board Outline: If there is the specific layer for board contour, give that layer name. This layer will be transferred to layer number 21 in PDB structure.
 - Drill Layer: If there is the specific layer for drill, give that layer name. This layer will be transferred to layer number 22 in PDB structure.
 - ③ **Signal Layer in Part Section**: In footprint definition, check this option if object layer is signal layer.

Signal Layer in Line Data Section: In board figure definition, check this option if object layer is signal.

Level 0 is Board Outline: Check this option if layer level 0 is board contour layer. **Allow Broken Component**: Check this option if Broken Component is used.

④ **COC of 0 Line Width**: Check this option if line width of COC as 0.

CAM Pad Over Size (Solder, Paste): Check this option if solder mask definition is recorded in CAM.

Generate Teardrops: This option is used automatically generated teardrop shape at PAD and Via.

Remove Duplicated Segments: Check this option to remove duplicated segments.

3.4. ODB++

ODB++ is ASCII format of Mentor Graphics to complement the weakness of GERBER format. Thus, it has all intelligent design information. PollEx PCB also supports this format. To import ODB++ file, use the following menu, **File > Import ECAD > ODB++**.

	Altium PCAD (*.pcb)	
	Altium Designer (*.PcbDoc)	
	Cadence - Allegro Expansion	
	Cadence Specctra, Cadence OrCAD	
	CADVANCE	
	Autodesk EAGLE (*.brd)	
	MentorGraphics - Board Station	
	MentorGraphics - <u>N</u> eutral File	
	MentorGraphics - Xpedition	
	MentorGraphics - PADS (*.asc)	
	ODB++	
	Zuken - Cadstar(*.cpa)	
	Zuken - CR5000 <u>B</u> oardDesigner	
	Zuken - CR5000 PWS	
	IPC-2581	
	CAM350	
	Gerber(RS-274D/RS-274X)	
6	Open Ctrl + O	
	Read PDB ASCII(*.pdba)	
	Read PDB XML(*.pdbx)	



		Import from ODB++		>
		3 Select Unit to be say	ved	
Import from ODB++	×	C mm	inch	C mi
Import from Compressed File (*.tgz, *tar.gz) Select Extraction Path 2.• Data Folder		Select Step	I Selected St	tep (including Sub-Board)
Next Cancel		Apply to Enviro	onment Setting	(4) User Defined Setting
		Imp	port	Cancel
		Reading and Conve	rting Status	

- ① **Compressed File:** Select ODB++ compressed file. Also, define additional option about uncompressing path. The folder is created in the uncompressing path.
- ② **Data Folder:** If the ODB++ file system exists as a folder structure, select the top level folder in hierarchical folder structure. Select top folder in folder searching dialog window.
- ③ Select Unit to be Saved: Specify the unit of PDBB, not the unit used in ODB++ design.
- ④ **User Defined Setting:** Enable user to specify parameters for data importing options.



3.5. Zuken Interface

PollEx PCB supports various Zuken's CAD design files, Cadstar, Board Designer and PWS.

3.5.1.1. Zuken - Cadstar (*.cpa)
Step1. Extract ASCII file from Zuken Cadstar.
Step2. Use the menu, File > Import ECAD > Zuken - Cadstar(*.cpa).



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	Altium PCAD (*.pcb)	
	Altium Designer (*.PcbDoc)	
	Cadence - Allegro Expansion	
	Cadence Specctra, Cadence OrCAD	
	CADVANCE	
	Autodesk EAGLE (*.brd)	
	MentorGraphics - Board Station	
	MentorGraphics - Neutral File	Import from Zuken Cadstar
	MentorGraphics - Xpedition	
	MentorGraphics - PADS (*.asc)	Cadstar ASCII File(*.cpa)
	ODB++	
	Zuken - Cadstar(*.cpa)	Import Cancel
	Zuken - CR5000 BoardDesigner	Reading and Converting Status
	Zuken - CR5000 PWS	
	IPC-2581	
	CAM350	
	Gerber(RS-274D/RS-274X)	
0	Open Ctrl + O	
	Read PDB ASCII(*.pdba)	
	Read PDB XML(*.pdbx)	

Select *.cpa and pressing OK button start reading Zuken CADSTAR design.

3.5.1.2. Zuken - CR5000 Board Designer

PollEx PCB can read Zuken BD (Board Designer) ASCII file. Upon using the utility, user can extract ASCII file from Zuken BD's binary design, *.pcb.

Step1. ASCII files extraction using utility command, BDExtractor.exe.

PollEx PCB supports two types of board types, single and arrayed board to read Zuken Board Designer. Array board file, *.pnf should have single boards information in it and at same time, single board files, *.pcf should also exist at certain folder.



To get ASCII file from Zuken BD, use the utility command, BDExtractor.exe.

Using this command, user can extract single and array board. File location is under C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share\BDExtractor.exe.



BDExtractor	_		×
*.pcb			
		Ok	Cancel

After specifying design file, *.pcb, press the OK button to start ASCII file extraction.

Step2. Importing design into PollEx PCB using ASCII files.

Use the menu, File > Import ECAD > Zuken - CR5000 Board Designer.

	Altium PCAD (*.pcb)		
	Altium Designer (*.PcbDoc)	Import from Zuken CR5000 Board Desinger	×
	Cadence - Allegro Expansion	1 Reading Board Selection	
	Cadence Specctra, Cadence OrCAD	C Arrayed Board © Single Board	
	CADVANCE	Board Contour Layer Name Setup	
	Autodesk EAGLE (*.brd)	Single Board BOARD_FIGURE	
	MentorGraphics - Board Station	Arrayed Board(PNF) BOARD_FIGURE	
	MentorGraphics - Neutral File	Check Board Layer Name Spelling	
	MentorGraphics - Xpedition	Display only One for the Same Boards in Arrayed Board	
	MentorGraphics - PADS (*.asc)		
	ODB++		-
	Zuken - Cadstar(*.cpa)		
	Zuken - CR5000 BoardDesigner	Convert closed Polyline to Polygon shape	
	Zuken - CR5000 PWS	Save This Structure As Default	
	IPC-2581		
	CAM350	Board Designer ASCII File (*.PCF, *.PNF)	<u>,</u>
	Gerber(RS-274D/RS-274X)	Import Cancel	
6	Open Ctrl + O	Reading and Converting Status	
	Read PDB ASCII(*.pdba)		-
	Read PDB XML(*.pdbx)		

- 1 3 Select the board type between Arrayed Board and Single Board.
- ② For the single and arrayed board, user can define the layer name of board contour layer. Then, user can also define the rule to read as many as number of single boards or just one for same type board during arrayed board reading case.
- ③ Specify the layer name in Board Designer to be used with hole data layer in PDB.
- ④ PollEx PCB read 2 ASCII files, *.pcf and *.ftf, but it is enough to specify with *.pcf. PollEx PCB automatically find *.ftf file in the same folder. For reading arrayed board, another two files, *.pnf and *.ftf, are necessary.

3.5.1.3. Zuken - CR5000 PWS

PollEx PCB supports two types of reading, artwork and wiring modes for Zuken PWS. Artwork mode means that all objects in design have no intelligent information like net name. All routing patterns exist on physical layers, but they don't have net information, so they will be transferred to just graphic data. In this case, after reading design with artwork mode, user cannot use these designs for nets related function or for electrical analysis.

*.BSF	Board specification information file.
*.CCF	Net information file.
*.MDF	Part information file.
*.UDF	Component placement and board graphic information file.
*.WDF	Routing pattern information file.

All needed ASCII files are following 5 files.

Step1. Extract ASCII file from Zuken CR5000 PWS. Step2. Use the menu, **File > Import ECAD > Zuken – CR5000 PWS.**

	Altium PCAD (*.pcb)		
	Altium Designer (*.PcbDoc)		
	Cadence - Allegro Expansion	Hand for Take Bill	
	Cadence Specctra, Cadence OrCAD	Top / Bottom Layer	
	CADVANCE	Silk Mark	
	Autodesk EAGLE (*.brd)	Assy's / Sik-2	×
	MentorGraphics - Board Station	Solue: Mask	v ق Search Zuken PWS ک
	MentorGraphics - Neutral File	Paste Mask Organize Vew folder	Date modified
	MentorGraphics - Xpedition	Board Hole # Quick access test.of	12/24/2010 6:16 PM BSF File 10/1/2010 9:59 AM CCF File
	MentorGraphics - PADS (*.asc)	In case of not using board contour layer specified in BSF This PC test.mdf This PC test.mdf test.mdf test.mdf	12/27/2010 10:24 AM MDF File 12/27/2010 10:24 AM UDF File 12/27/2010 10:24 AM WDF File
	ODB++		
	Zuken - Cadstar(*.cpa)	- Exclude Layers	
	Zuken - CR5000 BoardDesigner	Load ZLS Fie Save As Fie	
	Zuken - CR5000 PWS	Apply to Environment Setting Filegume	ZUKNE PWS file(*.bsf; *.ccf; *.m ~
	IPC-2581	PWS ASCII Fée (*.bsf)	<u>Qpen</u> Cancel
	CAM350	Reading and Converting Status	
	Gerber(RS-274D/RS-274X)		
0	Open Ctrl + O	Import Cancel	
	Read PDB ASCII(*.pdba)		
	Read PDB XML(*.pdbx)		

Among the 5 files, select any one of them and PollEx PCB can detect all other files and automatically read design.



To define usage of artwork layers in PWS, it is preferred to define all top/bottom corresponding layers. Depending on users, they are using different layer mapping tables in BSF. These layers mapping status can be saved into file, *.zls and re-use it for the next reading.



3.6. IPC-2581 Interface PollEx PCB supports IPC-2581 file such as *.cvg file.

Altium PCAD (*.pcb)	
Altium Designer (*.PcbDoc)	
Cadence - Allegro Expansion	
Cadence Specctra, Cadence OrCAD	
CADVANCE	
Autodesk EAGLE (*.brd)	
MentorGraphics - Board Station	Import from IPC-2581B
MentorGraphics - <u>N</u> eutral File	
MentorGraphics - Xpedition	IPC-2581B XML File(*.xml)
MentorGraphics - PADS (*.asc)	Import Cancel
ODB++	
Zuken - Cadstar(*.cpa)	Reading and Converting Status
Zuken - CR5000 <u>B</u> oardDesigner	
Zuken - CR5000 PWS	
IPC-2581	
CAM350	
Gerber(RS-274D/RS-274X)	

3.7. CAM 350

Read PDB ASCII(*.pdba) Read PDB XML(*.pdbx)

PollEx PCB supports CAM350 file such as *.CAM file.

	Altium PCAD (*.pcb)	
	Altium Designer (*.PcbDoc)	
	Cadence - Allegro Expansion	
	Cadence Specctra, Cadence OrCAD	
	CADVANCE	
	Autodesk EAGLE (*.brd)	Import from CAM350 X
	MentorGraphics - Board Station	
	MentorGraphics - <u>N</u> eutral File	CAM350 ASCII File (*.CAM)
	MentorGraphics - Xpedition	,
	MentorGraphics - PADS (*.asc)	Linport Cancel
	ODB++	Reading and Converting Status
	Zuken - Cadstar(*.cpa)	
	Zuken - CR5000 <u>B</u> oardDesigner	
	Zuken - CR5000 PWS	
	IPC-2581	
	CAM350	
	Gerber(RS-274D/RS-274X)	
6	Open Ctrl + O	
	Read PDB ASCII(*.pdba)	
	Read PDB XML(*.pdbx)	



3.8. Gerber Data Interface

Read PDB XML(*.pdbx)

PollEx PCB supports four types of GERBER formats, 274X, 274D, Drill and Square Hole. When you import Gerber Data, PollEx PCB analyze the file format internally and separate to 274X, 274D, Drill file, Square Hole and Aperture.

In case of 274D, there are necessary both of Gerber data and Aperture file.

If there are multiple aperture files, PollEx PCB make to one aperture data based on D-Code.

Use the following menu, File > Import ECAD > Gerber(RS-274D/RS-274X).

Altium PCAD (*.pcb)				
Altium Designer (*.PcbDoc)				
Cadence - <u>Allegro</u> Expansion				
Cadence Specctra, Cadence	OrCAD			
CADVANCE				
Autodesk EAGLE (*.brd)		Import from Gerber(RS-274D/R	(S-274X)	
MentorGraphics - Board Stat	ion	Corbor ACCII File		
MentorGraphics - <u>N</u> eutral File		Gerber ASCII File		
MentorGraphics - Xpedition		Import		Cancel
MentorGraphics - PADS (*.as	sc)			
ODB++		Reading and Converting Sta	itus	
uken - Cadstar(*.cpa)				
Zuken - CR5000 <u>B</u> oardDesigr	her	1		
Zuken - CR5000 PWS				
PC-2581				
CAM350				
Gerber(RS-274D/RS-274X)				
Open	Ctrl + O			
Read PDB ASCII(*.pdba)				



4. Export To

4.1. PollEx ASCII Interface

PDBB file is PollEx PCB's binary design file including all geometries and entities necessary to describe whole PCB design. In addition, PollEx PCB provides same ASCII file structure, *.pdba. This is ASCII version of PDBA file.

Step1. Exporting design to ASCII file, *.PDBA in PollEx PCB. Use the menu, **File > Export To > PDB ASCII (***.pdba).

PDB ASCII (*.pdba) PDB XML (*.pdbx) Ansys Neutral (*.anf) Ansys SIwave (*.siw) Cadence Sigrity (*.spd) Keysight 3070 Keysight ADS (*.adfi) Keysight ABL (*.xml) Zuken Hot-Stage (*.rif) IPC-2581B (*.xml) Restricted PDBB DXF GDSII Image

After using above menu, at file saving dialog box, specify the file name and path to export into ASCII file.

Step2. Reading ASCII file, *. PDBA in PollEx PCB.

Export to PDB ASCII	×
PDB ASCII File (*.pdba)	₩PollExPCB₩PollEx_New_Sample.pdba
Export	Cancel
Exporting and Converting Status	

Select the file in dialog window and pressing OK button will start reading ASCII file, *.PDBA into PollEx PCB.



4.2. PDB XML(*.pdbx) Step1. Exporting design to XML file, *.PDBX in PollEx PCB. Use the menu, **File > Export To > PDB XML (*.pdbx).**

PDB ASCII (*.pdba)
PDB XML (*.pdbx)
Ansys Neutral (*.anf)
Ansys SIwave (*.siw)
Cadence Sigrity (*.spd)
Keysight 3070
Keysight ADS (*.adfi)
Keysight ABL (*.xml)
Zuken Hot-Stage (*.rif)
IPC-2581B (*.xml)
Restricted PDBB
DXF
GDSII
Image

After using above menu, at file saving dialog box, specify the file name and path to export into XML file.

Step2. Reading XML file, *. PDBX in PollEx PCB.

Export to PDB XML	×
PDB XML File (*.pdbx)	#PollExPCB#PollEx_New_Sample.pdbx
Export	Cancel
Exporting and Converting Status	

4.3. Export Design to EDA vendor's Formats

PollEx PCB supports exporting to other EDA vendors' format. Use the menus under command, **PollEx PCB > File > Export To**



PCB File Setting View Properties Tools Analysis Option Manufa Import ECAD ۲ Export To ۲ PDB ASCII (*.pdba) PDB XML (*.pdbx) Open Ctrl + O Ansys Neutral (*.anf) Save Ctrl + S Ansys SIwave (*.siw) Save As Cadence Sigrity (*.spd) Save As Project Keysight 3070 4 Print Ctrl + P Keysight ADS (*.adfi) × <u>C</u>lose Keysight ABL (*.xml) Recent Design File List • Zuken Hot-Stage (*.rif) IPC-2581B (*.xml) Exit Restricted PDBB DXF GDSII

Image

PollEx PCB can export 8 different types of EDA vendors. There are Ansys Neutral File, Ansys SIWave File, Cadence Sigrity File, Keysight 3070, Keysight ADS File, Keysight ABL File(XML), Zuken Hostage, IPC-2581B.

4.3.1. Ansys Neutral (*.anf)

Using this menu, user can export file to be used in Ansys Neutral. To do this work, use the menu, **File > Export To> Ansys Neutral (***.anf).

PDB ASCII (*.pdba)				
PDB XML (*.pdbx)			Parameter Settings	×
Ansys Neutral (*.anf)			Combine Figure by	Reference (Prefix)
Ansys SIwave (*.siw)			Reference	
Cadence Sigrity (*.spd)	Export to Ansys Neutral	×	Combine Net by Re Reference	ference (Prefix)
Keysight 3070 Keysight ADS (*.adfi)	Ansys Neutral File (*.anf) Parame	«₩PollExPCB₩PollEx_New_Sample.anf	Default Value	1e-12 F
Keysight ABL (*.xml)	Export	Cancel	Resistance Inductance	0.001 Ohm
IPC-2581B (*.xml) Restricted PDBB	Exporting and Converting Status		Passive Component Capacitance Resistance	(Prefix)
DXF			Inductance	L
GDSII			Transparency	
Image			OK	Cancel



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4.3.2. Ansys SIwave (*.siw)

Using this menu, user can export file to be used in Ansys SIWave. To do this work, use the menu, **File > Export To > Ansys SIWave (***.siw)

PDB ASCII (*.pdba)		
PDB XML (*.pdbx)		Parameter Settings ×
Ansys Neutral (*.anf)		Combine Figure by Reference (Prefix)
Ansys SIwave (*.siw)		Reference
Cadence Sigrity (*.spd)	Export to Ansys SIWave X	Combine Net by Reference (Prefix) Reference
Keysight 3070 Keysight ADS (*.adfi) Keysight ABL (*.xml) Zuken Hot-Stage (*.rif)	Ansys SIWave File (*.siw) x\PollExPCB\PollEx_New_Sample.six Parameter Settings Export Cancel Exporting and Converting Status	Default Value Capacitance 1e-12 F Resistance 0.001 Ohm Inductance 1e-09 H
IPC-2581B (*.xml)		Capacitance C
Restricted PDBB		Resistance AR, RA, R
DXF		Inductance L
GDSII		Transparency
Image		OK Cancel

4.3.3. Cadence Sigrity (*.spd)

Using this menu, user can export file to be used in Sigrity SPD. To do this work, use the menu, **File > Export To > Cadence Sigrity (***.spd).

	PDB ASCII (*.pdba)					
	PDB XML (*.pdbx)					
	Ansys Neutral (*.anf)					
	Ansys SIwave (*.siw)					
	Cadence Sigrity (*.spd)					
	Keysight 3070					
	Keysight ADS (*.adfi)					
	Keysight ABL (*.xml)					
	Zuken Hot-Stage (*.rif)					
	IPC-2581B (*.xml)					
	Restricted PDBB					
	DXF					
	GDSII					
	Image					
		-		Parameter Settings		
				Transient Description Parameters		Mesh Line Parameters
Exp	ort to Cadence Sigrity		×	Final Time Time Steps	100	Mesh X 30 Mesh Y 30
			- 1	View Steps	10	Objects Color Setup
Cad	Jence Sigrity File (*.sig)	PollExPCBWPollEx_New_Sample.spc	•	DC Window	NO • YES •	Hole_Color YELLOV VIa_Color RED Hole_Color YELLOV Plane_Color GREEN
				Int Method		

			Time Steps	100	Mesn X 30 Mesn Y	30
adence Sigrity File (*.sig)			View Steps DC Window	10 NO • YES •	Objects Color Setup Trace_Color BLUE Via_Col Hole_Color YELLOV Plane_	lor RED Color GREEN
Paramete	r Settings –	h	Int Method Plane Skin Effect	TRAPEZOID	Default Layer Setup Conductive Layer Thickness	0.035
Export	Cancel		Stc_SPD_Transmission Line	NO •	Dielectric Layer Thickness	0.1
Exporting and Converting Status			Inter Plane Coupling Passivity Check	NO T	Permittivity Value LossTangent Value	4.3
			Dielectric Loss Dispertion Fmax_Transmission Line IBIS_Transition_Control	NO		
		1		OK 10	Cancel	

4.3.4. Keysight 3070

Using this menu, user can export file to be used in Keysight 3070. To do this work, use the menu, **PollEx PCB > File > Export To > Keysight 3070.**



PollEx PCB supports AGILENT i3070 format and also exports location report for test point.

	PDB ASCII (*.pdba)						
	PDB XML (*.pdbx)						
	Ansys Neutral (*.anf)						
	Ansys SIwave (*.siw)						
	Cadence Sigrity (*.spd)						
	Keysight 3070						
	Keysight ADS (*.adfi)						
	Keysight ABL (*.xml)						
	Zuken Hot-Stage (*.rif)						
	IPC-2581B (*.xml)						
	Restricted PDBB						
	DXF						
	GDSII						
	Image						
				Parameter Settings			×
				Bypass Set Card Option			
Exp	port to Keysight 3070	×		Component Set Device Option Family Option Global Option Notifies Set	Select Power Net-		
Ke	ysight 3070 File Path			- TP Define Set - Tooling Set - Constrainsts Set	Select Ground Net		
C	Parameter Se	ettings	L				
	Export	Cancel					
E	xporting and Converting Status						
				Save Load		OK Cancel	

4.3.5. Keysight ADS File

Using this menu, user can export file to be used in Keysight ADS. To do this work, use the menu, **PollEx PCB > File > Export To > Keysight ADS (***.adfi).

PDB ASCII (*.pdba)		
PDB XML (*.pdbx)		
Ansys Neutral (*.anf)		
Ansys SIwave (*.siw)		
Cadence Sigrity (*.spd)		
Keysight 3070	Export to Keysight ADS	×
Keysight ADS (*.adfi)	Keysight ADS File (* adf)	
Keysight ABL (*.xml)	Reysigne Abs the (Tadity	
Zuken Hot-Stage (*.rif)	Export	Cancel
IPC-2581B (*.xml)	Eventing and Converting Status	
Restricted PDBB	Exporting and Converting Status	
DXF		
GDSII		
Image		

4.3.6. Keysight ABL (*.xml)

Using this menu, user can export file to be used in Keysight ABL. To do this work, use the menu, **PollEx PCB > File > Export To > Keysight ABL (*.xml).**



PDB ASCII (*.pdba)			
PDB XML (*.pdbx)			
Ansys Neutral (*.anf)			
Ansys SIwave (*.siw)	Export to Keysight ABI		×
Cadence Sigrity (*.spd)	Export to Reysignt Abe		~
Keysight 3070	Keysight ABL File (*.xml)	×	₩PollExPCB₩PollEx_New_Sample.xm
Keysight ADS (*.adfi)	Evert		Canad
Keysight ABL (*.xml)	Export		Cancel
Zuken Hot-Stage (*.rif)	Exporting and Converting Status	;	
IPC-2581B (*.xml)			
Restricted PDBB			
DXF			
GDSII			
Image			

4.3.7. Zuken Hot-Stage (*.rif)

Using this menu, user can export file to be used in Zuken Hotstage. To do this work, use the menu, **PollEx PCB > File > Export To > Zuken Hot-Stage (*.rif)**.

PDB ASCII (*.pdba)			
PDB XML (*.pdbx)			
Ansys Neutral (*.anf)			
Ansys SIwave (*.siw)		7	
Cadence Sigrity (*.spd)	Export to Zuken Hot-Stage X	ł.	Parameter Settings X
Keysight 3070	Zuken Hot-Stage File(*.rif)		Parameter Control
Keysight ADS (*.adfi)	Parameter Settings	١.	Export Unit
Keysight ABL (*.xml)	Export Cancel	1	- Unit mm 👻
Zuken Hot-Stage (*.rif)	Exprting and Converting Status		- Precision(Integer) 0
IPC-2581B (*.xml)			Cancel
Restricted PDBB			L
DXF			
GDSII			
Image			



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4.3.8. IPC-2581B

Using this menu, user can export file to be used in IPC-2581. To do this work, use the menu, **PollEx PCB > File > Export To > IPC-2581B.**

PDB ASCII (*.pdba)	
PDB XML (*.pdbx)	
Ansys Neutral (*.anf)	
Ansys SIwave (*.siw)	
Cadence Sigrity (*.spd)	Export to IPC-2581B X
Keysight 3070	IPC-2581B File (*.xml) C:\#Temp\#Altair-PollEx\#PollExPCB\#PollE
Keysight ADS (*.adfi)	
Keysight ABL (*.xml)	Export Cancel
Zuken Hot-Stage (*.rif)	Exporting and Converting Status
IPC-2581B (*.xml)	
Restricted PDBB	
DXF	
GDSII	
Image	

4.4. Restricted PDBB

Using this feature, user can save some parts of whole board, after selecting nets and connected components for selected nets. In case of sending design to outer but if users do not want to whole board with security issues, this feature is effective. Use the menu, **File > Export To > Restricted PDBB**.

PDB ASCII (*.pdba)
PDB XML (*.pdbx)
Ansys Neutral (*.anf)
Ansys SIwave (*.siw)
Cadence Sigrity (*.spd)
Keysight 3070
Keysight ADS (*.adfi)
Keysight ABL (*.xml)
Zuken Hot-Stage (*.rif)
IPC-2581B (*.xml)
Restricted PDBB
DXF
GDSII
Image

Upon launching **Restricted PDBB** menu, user meets following dialog menu to save partial design.





User has three options for saving design. One is saving component placement information only (1). Another is saving selected area only (2) and the other is saving design depending objects and related objects (3).

- ① Select **Export Component Only** button menu to save design for only components placement. At this status, routing and non-electrical information will be excluded at saving.
- ② **Export Selected Area Only** will give users two selection method. One is selecting rectangle area and the other is selecting arbitrary area.
- ③ Export by Object Selection Method will give users two selection menu windows. Combining two windows' selections, user can select objects. If Window 1 selection is Component, Window 2 selection will be Net and vice versa. It means user can select component and its connected net and vice versa.

Using **Search** button menu, user can find necessary objects in **Window 1**.

- Automatically include other connected components

If **Window 1** selection is Component, **Window 2** selection will be Net automatically. In this case, and if this checking is turn on status, PollEx PCB will save also save include other side component also.





- Show Composite Net Passive Component

If user selected components and they are connected with passive device, PollEx PCB will include passive device for saving when this option is turn on status.



- Select All

Select all items in Window 2.

- Display

Show selections on PCB Viewing Area.

- Exclude

Show selections on PCB Viewing Area with hidden for unselected objects.

- Clear

Reset window display.

④ Exporting Options

- Initialize stack-up information

Reset stack-up information and make it with default value.

- Initialize Artwork Layer information

Reset artwork layer information and make it with default value.

- Remove Board-Contour

Remove board contour data and make it with basic rectangle geometries.

- Initialize Component Name

Remove all part's name information and rename them with string starting "PartXXX". All other footprint, package and device name will be re-arranged. Vias and padstacks name will be re-arranged also.

- Initialize Net Name

Remove all nets' name and rename them with string starting "NetXXX". Vias and padstacks name will be re-arranged also.

- Initialize Net/Component Property

Remove all properties assigned to net and components (reference designator).

- Include Component Outline

Include all component outline of component (Artwork Layer-201: COC Top, 202: COC Bottom).

- Include Solder Mask



Include all solder mask layer.

- Include Metal Mask

Include all metal mask layers.

- Include Board Figure

Include all board figures.

- Include Mechanical Objects

Include all mechanical objects.

- Include Comp Figure

Include all Component Figure Data.

5 Using **Save As** menu, save current status into different PDBB file.

4.5. DXF

Using this menu, user can export file to be used in DXF. To do this work, use the menu, **PollEx PCB** > **File** > **Export To** > **DXF**.



4.6. GDSII

Using this menu, user can export file to be used in GDSII Format. To do this work, use the menu, **PollEx PCB > File > Export To > GDSII.**

PDB ASCII (*.pdba)
PDB XML (*.pdbx)
Ansys Neutral (*.anf)
Ansys SIwave (*.siw)
Cadence Sigrity (*.spd)
Keysight 3070
Keysight ADS (*.adfi)
Keysight ABL (*.xml)
Zuken Hot-Stage (*.rif)
IPC-2581B (*.xml)
Restricted PDBB
DXF
GDSII
Image



Export to GDSII X	:	Add Output Layer X
Cutput Layer Setting		Format GDS2 Binary File (*.gds)
Selected Layer Output File Name Output Options		Select Layers :
		Output Options
Add Output Layer Export Cancel Exporting and Converting Status		Options for conversion from ARC to Separated LINE Divide Type : Angle C Length Divide Value : 10
		Cancel

4.7. Image

Using this menu, user can export Image file as * jpg or *.bmp. To do this work, use the menu, **PolIEx PCB > File > Export To > Image.**

PDB XML (*.pdbx) Ansys Neutral (*.anf) Ansys SIwave (*.siw) Cadence Sigrity (*.spd) Cadence Sigrity (*.spd) Keysight 3070 Keysight ADS (*.adfi) Keysight ABL (*.xml) Zuken Hot-Stage (*.rif) IPC-2581B (*.xml) Restricted PDBB DXF GDSII Image Image September 2 Image September 2 Cancel	PDB ASCII (*.pdba)	Export to Image	\times
Ansys Neutral (*.anf) ① Export Layer Setup Ansys SIwave (*.siw) ② Image Type Cadence Sigrity (*.spd) ③ JPG Keysight 3070 ③ Color Type Keysight ADS (*.adfi) ⑥ Color Type Zuken Hot-Stage (*.rif) PC-2581B (*.xml) Restricted PDBB DXF GDSII ⑤ Export Image ⑤ Export	PDB XML (*.pdbx)		
Ansys SIwave (*.siw) 2 Image Type Cadence Sigrity (*.spd) Image Type Keysight 3070 Image Type Keysight ADS (*.adfi) Image Type Keysight ADS (*.adfi) Image Type Keysight ADS (*.adfi) Image Type Zuken Hot-Stage (*.rif) Image Size IPC-2581B (*.xml) Image Size DXF Dimension GDSII Sexport Image Sexport	Ansys Neutral (*.anf)	 Export Layer Setup 	
Cadence Sigrity (*.spd) Image Keysight 3070 Image Keysight ADS (*.adfi) Image Keysight ABL (*.xml) Image Zuken Hot-Stage (*.rif) IpC-2581B (*.xml) IPC-2581B (*.xml) Image Restricted PDBB Image DXF Image GDSII Image Image Image Image Image	Ansys SIwave (*.siw)	2 Image Type	
Keysight 3070 Keysight ADS (*.adfi) Keysight ABL (*.xml) Zuken Hot-Stage (*.rif) IPC-2581B (*.xml) Restricted PDBB DXF GDSII Image Image	Cadence Sigrity (*.spd)		
Keysight ADS (*.adfi) Keysight ABL (*.xml) Zuken Hot-Stage (*.rif) IPC-2581B (*.xml) Restricted PDBB DXF GDSII Image	Keysight 3070		
Keysight ABL (*.xml) Zuken Hot-Stage (*.rif) IPC-2581B (*.xml) Restricted PDBB DXF GDSII Image Sexport Cancel	Keysight ADS (*.adfi)	G Color	
Zuken Hot-Stage (*.rif) Image Size IPC-2581B (*.xml) Define a pixel size Dimension Keep Aspect Ratio Height 1024 Width 1920 Image Sexport	Keysight ABL (*.xml)	• Color • Monochrome	
IPC-2581B (*.xml) Restricted PDBB DXF GDSII Image	Zuken Hot-Stage (*.rif)	4 Image Size	
Restricted PDBB Image DXF Dimension GDSII Sexport Cancel	IPC-2581B (*.xml)	O Define a pixel size	
DXF GDSII Image	Restricted PDBB	Dimension Keep Aspect Ratio	
GDSII (S)Export Cancel	DXF	Height 1024 Width 1920	
Image	GDSII	Evport Cancel	
	Image	Cancer	

① **Export Layer Setup:** Select the layer(s) either artwork or physical layers to export by using 'Export Layer Setup' button.

🐉 Layer		× 🐹	Layer	×
Artwork Layer	Physical Layer		Artwork Layer	Physical Layer
V Name	Layer	^		Export Only Conductive Layer
TOP Pad + Pattern	1, 2	V	Name	Layer
BTM Pad + Pattern	11, 12		1	1, 2, 4, 5
	1		2	81
padstack top	2		3	82
Resist-A	3		4	83
C Symbol-A	4		5	84
Symbol-A-1	5		6	11, 12, 14, 15
MetalMask-A	6			
HeightLimit-A	7			
inhibit(plc)-A	8			
inhibit(plc)-C	9			
inhibit(wir)-A	10			
□ 6	11			
padstack bottom	12			
C Resist-B	13			
Symbol-B	14			
Symbol-R-1	15	~		
OK	Cancel		OK	Cancel

If you select physical layer, 'Export only conductive layer' menu will be enable to include.

② **Image Type:** Select the file type as JPG or BMP.



- 3 **Color Type:** Select a color type as Color or Monochrome.
- (4) **Image Size:** Set the image size.
- Define a pixel size: Set an each pixel size.
 Ex.) If you have a board size as 100x100, and then set the value as 0.1. It will be exported as 1000x1000. (The current unit in PCB design will be used.)
 Dimension: Set the image size according to given resolution value as Height and Width.
 Keep Aspect Ratio: By using this option, the image size will be calculated automatically with considering actual board size and given dimension value.
- **Export:** You can get the exported image with clicking this button.

5. Print

PollEx PCB's print feature supports three types of formats.

- 5.1. Bitmap
- Use the menu, **File > Print**.

Print Paper Size Ratio Size ratio regarding to the PCB. **Quality**: The scale of resolution.



5.2. PostScript

To print out postscript file, use the menu, **File > Print**. **Real Size**: Print out size as same as the real PCB size. **Complementary Color**: Define the color of printing. **Current View Area**: Print out same as viewing status.



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Print Option	×
C BitMap Print to file	
Print Paper Size Ratio	
© 100% C 75% C 50% C 25%	
C User 100	
- Quality	
C High C Medium 💿 Low	
Real Size Complementary Color Current View Area	ſ
C PDF Output Layers C Current View Layer (1 Page only) C Select Layers	
- Size & Orientation Paper Size A4	
© Portrait C Landscape	
OK Cancel	

5.3. PDF

To print out with PDF format, use the menu, **File > Print**. **Paper Size**: Select the paper size.





Setting

Under the setting menu, there are many setting items for defining default value for using PollEx PCB. Use the menus under **Setting** in main menu.

<u>S</u> ett	ting	<u>V</u> iew	Properties	
	<u>E</u> nv	<u>E</u> nvironment		
s;	Layer		Alt + L	
	Measure			
\searrow	<u>P</u> icking			
	Unit Conversion			
8	Board Information			

1. Environment

Using this menu, users can set-up defaults for using PollEx PCB. Setting items are as follows;

- Whether user set password during saving operation for design open
- Working file path
- Display method
- Default language for menu and manual
- Default setting for different ECAD reader

Use the menu, **Setting > Environment**.



20 Environment			
General 1	Default search Directory	2	
Layer Initial View Status Layer Stack Tool Picking	Log file (*.log) path PDBB Encryption Excel Export Default save directory C. W InsertMan Juny 2014	C: WUsers Weunkyoung WAppData WRoaming W	
PCB Explorer Component Arrangement Plan ECAD	File Format		•
Altium PCAD Altium Designer Cadence - Allegro Expansion CADVANCE MentorGraphics - Board Station, Neutra	Language Menu (Dialog) Window View Manual	English English English	•
	Auto-Update Use Auto-Update PollEx installation file directory		
···· Gerber ···· Analysis	Default net dass file path	C:\Users\Use	
Block Design Generator DEM / DEE / DEE + / DEA	Default material file path Default MPN reference file path	C: \Users veunkyoung \AppData \Roaming \ C: \Users veunkyoung \AppData \Roaming \	Ē
DFM DFE DFE+ DFA Component Mounting Emulator < >	Default part library directory		1

- ① Classification for environment setting items.
- ② Each item's parameter setting window.
- ③ User can load or save environment setting. So multiple users can share setting to use same environment.



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1.1. General

① **General**: User can set language and default file path.



- ② **Default search Directory**: Set default file open path for PollEx PCB.
- 3 Log File (*.log) path: Set default log file saving path.
- ④ **PDBB Encryption**: Define whether to use encryption when saving PDBB file. If user checks this option, user may meet following password input window before saving file.

ОК
Cancel

- ⑤ Excel Export: Set default MS/Excel export path and default export format such as csv, xls or xlsx.
- 6 **Language**: Default language for Menu, Window View and Manual is English.
- ⑦ **Auto Update**: Set default directory of Install file location.
- 8 **Default net class file path**: Set default net class file path.
 - Default material file path: Set default material file path.
 - Default MPN reference file path: Set default MPN reference file path.
 - Default part library directory: Set default part library directory.

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Save

1.2. View

① **View**: Set window display.

Environment	×
General	View
Initial View Status	Draw Mouse Cross Line Foreground Selected Route Hatched Display Fill Selected Route Diamond
Layer Stack Tool Picking PCB Explorer Component Arrangement Plan ECAD Altium PCAD Altium PCAD Altium Designer Cadence - Allegro Expansion CADVANCE MentorGraphics - Board Station, Neutra MentorGraphics - PADS (*.asc) ODB++ Zuken - CR5000 Board Designer Zuken - CR5000 Board Designer Zuken - CR5000 PWS Gerber Analysis Metal Mask Manager Block Design Generator DFM / DFE / DFE+ / DFA DFE DFE+ DFA Manufacture Component Muniting Emulator	Auto Zoom Fill Selected Route Zoom to Mouse Point Area Board Origin Mark Grid Set Capture Window Grid Size Selected Area Grid Size 100 mm Inch 0.1 DB Unit 0 Soom Factor 40 % Auto Zoom Scale 100 % Measurement Display Dimension Text Scale 100 % Number of Decimal 3 Vert Use CPU for graphic display operation (To apply this, restart PollEx.) Use Windows Operation (Zoom In/Out) Net Color Display 3D Board Color Setting
Component Mounting Emulator	

② **Draw Mouse Cross Line**: Mouse pointer shows with "+" mark.

Foreground Selected Route: During picking operation, selected pattern will be shown at the top if there are multiple patterns are overlapped.

OK

Cancel

Hatched Display: Display polygons to hatch as Forward Diagonal / Backward Diagonal / Cross / Diamond / Vertical /Horizontal.

Auto Zoom: Upon using PCB Explorer, Highlight or Exclude operation shows objects with auto zoom-in.

Fill Selected Route: Show selected routing pattern with filled shape.

Zoom to Mouse Point Area: Zoom area based on mouse point.

Board Origin Mark: Display the board origin mark

- ③ **Grid**: Set the distance of grid and decide whether PollEx PCB shows grid or not.
- ④ **Set Capture Window**: Use the menu to make partial image capture, screen capture, full area capture.
- 5 **Zoom**: Specify the zoom ratio.

Load

6 Measurement

Dimension Text Scale: Set the dimension's size using measure function.

Decimal Point: Set the decimal point for measure resulting. Select the value 1~5. **Display**: Select one among ceiling, round and floor for the decimal point.

⑦ Net Color Display: If source ECAD file has its original color settings for routing nets, this option will decide whether PollEx PCB show original ECAD color or use default PollEx PCB color.

User Windows Operation: For zoom In/Out and panning operation, operations will be applied reversely.



1.3. Layer - Initial View

① **Initial View**: Set the default PDBB file's open status for color, display and layer display on/off status.



② **Default Layer View**: Set layer's displaying status for top/bottom/inner layers. For the huge file size, checking top only is very effective for opening speed.

③ Display: For objects on PCB, set the objects showing status.
 Route On: Initially PollEx PCB display routing pattern.
 Component On: Initially PollEx PCB display components.
 Copper Fill: Initially PollEx PCB shows copper pour as filled shape.

- ④ **Physical Layer Definition**: Decide for showing top/bottom component related layer displaying status.
- ⑤ **Artwork Layer Color Setting**: PollEx PCB can define the artwork layers' default color. User can highlight some specific layers to change color.

1.4. Layer-Layer Stack

① **Layer Stack**: Set the PCB physical layer's composing materials.

Environment	(
···· View	Layer Stack			
	2 Material			
Initial View Status	9			
Layer Stack 1	Conductor	COPPER		-
- Tool				
Picking	Dielectric	FR4		•
PCB Explorer				
Component Arrangement Plan				
E-ECAD	(J) I hickness(mm)			
Altium PCAD	Conductor			
- Altium Designer	Top/Bottom	0.035	Inner	0.035
Cadence - Allegro Expansion	rop/bottom	0.055	11 In Ci	0.055
MenterCraphics - Reard Station Marth				
MentorGraphics - Xpedition	Dielectric			0.125
MentorGraphics - RADS (* asc)				
ODB++				
Zuken - CR5000 PWS				
Gerber				
Analysis				
Metal Mask Manager				
Block Design Generator				
DFM / DFE / DFE+ / DFA				
··· DFM				
··· DFE				
··· DFE+				
DFA				
- Manufacture				
Component Mounting Emulator				
>				

- ② **Material**: Define the PCB's conducting and di-electric material from material library.
- ③ **Thickness**: Define the conducting layer's default thickness values.

1.5. Tool - Picking

① **Picking**: Set the default parameter for using picking tool.

2 Environment		×
···· General ···· View	Picking	
- Layer Initial View Status Layer Stack - Tool - Picking 1 - PCB Explorer - Component Arrangement Plan - ECAD		
Altium PCAD Altium Designer Cadence - Allegro Expansion CADVANCE MentorGraphics - Board Station, Neutra MentorGraphics - Xpedition MentorGraphics - ADAS (*.asc) ODB++	Component Height Component Height Ver-Text Rotation Ver-Text Rotation	
Zuken - CR 5000 Board Designer Zuken - CR 5000 PWS Gerber Analysis Metal Mask Manager Block Design Generator Desch (DES 4054)	Display Component Information Reference Name Text Scale 100 % Pin-Connected Net Name	
Component Mounting Emulator	Selection Priority	C Route
Save Load	ОК	Cancel

- ② **Component**: Display what attributes are displayed when picked a component.
- ③ **Route**: Display what attributes are displayed when picked a route.

④ Display Component Information

Reference Name: Specify whether to show reference name in picking tool operation. **Pin Number**: Specify whether to show pin number in picking tool operation. **Pin-Connected Net Name**: Specify whether to show pin-connected net name in picking tool operation.

Text Scale: Set text scale.

5 Select Priority: Select priority among component, pin and route.





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1.6. Tool - PCB Explorer

① **PCB Explorer**: Set the default value for using PCB Explorer.

20 Environment		
General	PCR Evolorer	
···· View		
E-Layer	2) Initial Setup Option	
Initial View Status	Start Up PCB Explorer	
Layer Stack		
	Default Selection	
	Default Selection Type A	
Component Arrangement Plan	3 Default Selection Type A	
	Part C Ref C Net	
Altium PCAD		
Altium Designer	Display the placed Layer	
Cadence - Allegro Expansion		
CADVANCE	4 Default Selection Type B	_
- MentorGraphics - Board Station, Neutra	None C Part C Ref C Net	
	server sorrer sorrer	
MentorGraphics - PADS (*.asc)		
ODB++	S Part Name Type	
Zuken - CR5000 Board Designer	C Part Name ECAD Part Name	
Zuken - CR 5000 PWS	so renormente	
···· Gerber		
···· Analysis		
Metal Mask Manager		
Block Design Generator		
DFM / DFE / DFE + / DFA		
··· DFM		
DFE		
DFE+		
DFA		
E- Manufacture		
Component Mounting Emulator		
× /		
Save Load	OK Car	ncel

② **Initial Setup Option**: If this option is checked, PCB Explorer will be launched after opening PollEx PCB job file.



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PCB Explorer ×
Selection Type - A
Search Search
Part C Ref C Net
47151-0001 ▲ 675031020 ▲ AB38T-32.768KHZ ▲ ASFL1-16MHZ ■ BOOT_MODE ■ BSS123 ③ CICOSP121NC CLOSF103ZB5NNNC CL05F103ZB5NNNC CL055103ZB5NNNC CL055103ZB5NNNC ▼ Clear Color Excl Disp ■
Link All Contrast
© Or C And
Selection Type - B
None
C Part C Ref C Net
4
Sel All Color Exd Disp

- ③ Set the default selection Type A when launched the PollEx Explorer.
- 4 5 Set the default selection Type B when launched the PollEx Explorer.
- (5) In PDB data structure, there are two name properties, part name and ECAD part name. If there is broken component case, unique identifier, part name will be given differently than that is assigned in ECAD tools. Decide what name will be used in part selection window.

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1.7. Tool – Component Arrangement Plan

- ① **Component Arrangement Plan**: Set the default values for using the Component Arrangement Plan tool.
- 2 **Default Environment Setting**: Set environment file, *.cpas and input file path.





1.8. ECAD - Altium PCAD

- ① **Altium PCAD**: Default environment setting to import Altium PCAD.
- ② **Layer Set-up**: Set Altium layers' name which will be used as PDB's component outline layer and board outline layer.

Environment	×
General	Altium PCAD
General Status 	Altium PCAD COC (Place Boundary) Top COC (Place Boundary) Bottom Board Outline
Save Load	OK Cancel



1.9. ECAD - Altium Designer

- ① **Altium Designer**: Default environment setting to import Altium Designer.
- ② **Encoding**: Check this option if converting EUC-JP to Shift JIS.
- ③ **Layer Set-Up**: Set Altium layers' name which will be used as PDB's component outline layer and board outline layer.

20 Environment				×
General	^	ally man		
···· View		Altium Designer		
🖃 Layer	0	Encoding		
···· Initial View Status		Convert FLIC-1P to Shift 1IS		
Layer Stack				
	G	Layer Set-Up		
Picking		COC (Place Roundary) Top	Default	
···· PCB Explorer		COC (Flace boundary) Top	Derault	
Component Arrangement Plan		COC (Place Boundary) Bottom	Default	
E ECAD		Reard Outline	Default	
Altum PCAD		board Oddine	Derduit	
Altum Designer				
Cadence - Allegro Expansion				
Master Crashing Read Station Newton				
MentorGraphics - Doard Station, Neutra				
MentorGraphics - Apediuon				
ODB++				
Zuken - CR 5000 Doard Designer				
Gerber				
Analysis				
Metal Mask Manager				
Block Design Generator				
DFM / DFE / DFE + / DFA				
DFM				
DFE				
··· DFE+				
DFA				
🗄 Manufacture				
···· Component Mounting Emulator	~			
< >				
Save Load				OK Cancel



1.10. ECAD - Cadence Allegro Expansion

Cadence Allegro doesn't support ASCII out feature, but support command utility, extracta.exe. The extracta.exe is impossible to run alone. It require Allegro installation environment. But it does not ask any license.

① **Cadence Allegro Expansion**: Default environment setting to import Cadence Allegro design for support abnormal pads.



2 **Encoding:** while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

③ Import Type

Read from Binary File: Support default as Allegro binary file reading. **Read from ASCII File**: Support default as Allegro ASCII file reading.

Read form Fabmaster File: Support default as Allegro Fabmaster file reading.

④ Binary Reading Option

Path to the extra.exe: Set the file path for Allegro ASCII extraction command utility, extracta.exe. In general case, this file location is <code>%ALLEGRO_INSTALL_PATH% \tools\pcb\bin</code>.

Path to the Control File: set the path for Allegro ASCII extraction command control file, AllegroExpansion_ExtractCommandFile163.txt. In general case, this file is in C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Share\AllegroExpansion_Ex tractCommandFile163.txt.

- Allow Break Component: Check when user wants to import Break Component.
 Higher than Version 16.3: check this option while reading upper Allegro version than 16.3.
- 6 **Layer Set-Up**: Set Allegro layers' name which will be used as PDB's component related layers for silkscreen, component outline layer.



1.11. ECAD - CADVANCE

- ① **CADVANCE**: Set default value for reading design from CADVANCE file.
- ② **Layer Set-Up**: Set CADVANCE layers' name which will be used as PDB's component related layers for board outline layer.

😥 Environment	×
General	CADMANICE
··· View	CADVANCE
- Layer	
···· Initial View Status	Z Layer Set-Op
Layer Stack	Board Outline
Picking	Except Layer
PCB Explorer	
Component Arrangement Plan	
ECAD	
Altium PCAD	
Altium Designer	
Cadence - Allegro Expansion	
CADVANCE 1	
MentorGraphics - Board Station, Neutra	
MentorGraphics - Xpedition	
MentorGraphics - PADS (*.asc)	
ODB++	
Zuken - CR5000 Board Designer	
Zuken - CR5000 PWS	
Gerber	
Analysis	
···· Metal Mask Manager	
Block Design Generator	
DFM / DFE / DFE+ / DFA	
DFM	
DFE	
···· DFE+	
DFA	
- Manufacture	
Component Mounting Emulator 🛛 🗸	
< >	
Save Load	OK Cancel



1.12. ECAD - Mentor Board Station, Neutral

① **MentorGraphics Board Station, Neutral**: Set default value for reading design from Mentor Graphics Board-Station file.



- ② Encoding: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.
- **3 Board Type**

Single: Single board reading.

Array-Single Board: Arrayed board reading but for same type board, read one. **Array-Full Board**: Arrayed board reading.

- ④ **Copper Shape**: For Board-Station design's copper line, decide whether display overlapped dummy line or not.
- Add Drawing Part to Reference Designator: Add drawing data as part.
 Exclude Silkscreen of 0 Line Width: Excludes silkscreen having a line width of zero.
 Include Hatched Copper: Check this option if the hatched copper is used in the design.
- 6 **Layer Set-Up**: Set Mentor Graphics Board-Station and Neutral files layers' name which will be used as PDB's component related layers for component outline layer.
- Neutral File I/F Mode: Set the interface mode for Neutral files.
 Whole Files: Read all of files.
 Neutral Only: Read the component section only.



1.13. ECAD - MentorGraphics Xpedition

① **MentorGraphics Xpedition**: Set the default reading parameter for Mentor Graphics Xpedition design.

20 Environment		×			
General	MantarCraphics Vacdition				
···· View	Mentordraphics - Apeution				
⊡ · Layer	2-Encoding				
···· Initial View Status					
Layer Stack	Convert EUC-JP to Shift JIS				
···Picking	Opuons				
PCB Explorer	- Read sub-board				
Component Arrangement Plan	ASCII File Directory \$PCB\U00ftOutput\U00ftExpo	rtDesignData			
E ECAD	3				
Altum PCAD	Select Sub Board 🔽 Read only One for the Same Boards				
Altum Designer					
Cadence - Allegro Expansion					
CADVANCE	4 Allow Broken Component Allow Unconnected Net Rem	ove Net Data			
MentorGraphics - Board Station, Neutra					
MentorGraphics - Apeoluon	5 Layer Set-Up				
ODB	COC (Place Boundary) Top				
	COC (Place Boundary) Bottom				
Gerber					
Analysis	Board Outline BOARD_OUTLINE				
Metal Mask Manager					
Block Design Generator	Panel Outline PANEL_OUTLINE				
P. DFM / DFE / DFE + / DFA					
DFM	Hole Hole				
DFE					
··· DFE+					
DFA					
Manufacture					
Component Mounting Emulator 🗸 🗸					
< >					
Save Load	OK	Cancel			

- ② Encoding: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.
- ③ **Read sub-board**: Check this option when board is arrayed board.

User Defined ASCII Directory: If there is sub-board in array board, define the location of sub board file data.

Select Sub Board: Option to read the Sub Board.

Read only One for the Same Boards: Only read one board if there are same multiple boards.

④ **Allow Broken Component**: Check this option when user wants to convert referencechanged component to break component.

Allow Unconnected Net: Check this option when user wants to read unconnected net together.

Remove Net Data: Use this option when user wants to import design without routing information.

Layer Set-Up: Set Mentor Graphics layers' name which will be used as PDB's component related layers for component outline layer, board outline layer.



1.14. ECAD - PADS

① **MentorGraphics PADS**: Set the default reading parameters for Mentor Graphics PADS design.

20 Environment			×
General View	^	lentor - PADS	
- Layer	0	Laver Set-Up	
Layer Stack	(E	COC (Place Boundary) Top	
		COC (Place Boundary) Bottom	
PCB Explorer		Board Outline	
Component Arrangement Plan		Drill Layer	
Altium PCAD		Solder Mask Top	
		Solder Mask Bottom	
···· CADVANCE ···· MentorGraphics - Board Station, Neutra		Metal Mask Top	
MentorGraphics - Xpedition		Metal Mask Bottom	
···ODB++		Silk Bottom	
Zuken - CR5000 Board Designer Zuken - CR5000 PWS		Signal Layer in Part Section	Signal Layer in Line Data Section
···· Gerber ···· Analysis	3	Level 0 is Board Outline	Allow Broken Component
Metal Mask Manager		Options	
Block Design Generator DFM / DFE / DFE+ / DFA		COC of 0 Line Width	CAM Pad Over Size (Solder, Paste)
DFM DFE	4	Generate Teardrops	Remove Duplicated Segments
DFE+			
	、		
< >			
Save Load			OK Cancel

- ② **Layer Set-up**: Set specific purpose layer names which are used in PADS design. To use in DFM for component's measuring base, it is recommended to set all parameters here.
- ③ **Signal Layer in Part Section**: In footprint definition, check this option if object layer is signal layer.

Signal Layer in Line Data Section: In board figure definition, check this option if object layer is signal.

Level 0 is Board Outline: Check this option if layer level 0 is board contour layer. **Allow Broken Component**: Check this option if Broken Component is used.

④ **COC of 0 Line Width**: Check this option if line width of COC as 0.

CAM Pad Over Size: Check this option if solder mask definition is recorded in CAM.



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1.15. ECAD - ODB++

① **ODB++**: Set default value for reading design from ODB++ file.



- 2 Select Unit to be Saved: Select unit.
- ③ **Import from**: Select file type.

Compressed File: Compressed file type.

Data Folder: Folder type after decompressed.

④ Select Step

All: Read all design data

Selected Step(Including Sub-Board): Read only selected step design data

Use Multiple Threads: PollEx can support multi-treads when import file. Default is off mode.

Write Log File: Select this option to write a log history into *.log file.

Use the Origin point of the selected Step data: When this option is checked, use the origin point of the design data.

Skip Reading in Miscellaneous Data: Except to import Miscellaneous Data.

Separate Step Layers: Adding a step name at the end of the layer name when the design has step data.

User-defined Layer other than Default Layers: Read user defined layer file that defined layers to include or exclude.

Reload Layer Data(Applicable Only for Non-Intelligent data): This option is only applied to Legacy 32bit version. When the 32bit program cannot read big ODB++ data, this option creates a separate file per each layer.

Convert Drill to VIA: If Via hole describe in Drill layer, select this option to convert Drill to Via.

Add the Sub-board to specific Polygon Layer when Importing Panel data: When reading the upper level of ODB Step structure and including sub board, polygon is generated


by sub board outline shape.

Property title used for Pin Pad: The objects which have a same property are combined as one pad shape. (ex.".geometry")

Property title used for Route Pattern: The objects which have a same property are combined as one net. (ex.".net_name")

1.16. ECAD - Zuken CR5000 Board Designer

① **Zuken CR5000 Board Designer**: Set the default reading parameters for Zuken CR5000 Board-Designer design.

20 Environment		×
General View D-Layer Layer Status Layer Stack D-Tool Diction	Zuken - CR5000 Board Designer	
- PCB Explorer - Component Arrangement Plan	C Arrayed Board	Single Board
ECAD (4)	Board Contour Layer Name Setup	BOARD_FIGURE
···· Cadence - Allegro Expansion ···· CADVANCE	Arrayed Board(PNF)	BOARD_FIGURE
MentorGraphics - Board Station, Neutra MentorGraphics - Xpedition	Check Board Layer Name Spelling	Arrayed Board
	User Defined Hole Layers	
Gerber Analysis	Convert closed Polyline to Polygon Shape	e
	Board Designer Teardrop Generating Method Make using two Lines Make using two Lines and fill with Polygo	n
DFE+	 Display Option I → Display meshplane to solid plane 	
< Component Mounting Emulator		
Save Load		OK Cancel

② **Encoding**: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.

③ Reading Board Selection

Array Board: Check this option to read arrayed board. PollEx PCB will read $\star.pnf$ and $\star.ftf$ file.

Single Board: Check this option to read single board. PollEx PCB will read *.pcf and *.ftf file.

④ **Board Contour Layer Name Setup:** Set here the board contour layer name for single and arrayed board.

Check Board Layer Name Spelling: When this option is checked, PollEx PCB will check the specified name and if there is no matching layer, show the warning message to users.

Display only One for the Same Boards in Arrayed Board: When user imports arrayed board and if there are same type board, PollEx PCB will shows only one board shape for multiple board.

User Defined Hole Layers: When user used different name of hole layer, specify the layer name here.



- 6 Board Designer Teardrop Generating Method: There is not defined for tear drop shape in Zuken Board Designer's ASCII file because we have to create tear drop shape based on user selection. Select either Make using two Lines or Make using Lines and fill with Polygon.
- ⑦ Display Option: When this option is checked, after importing design, show meshed plane shape with same as solid plane.
- 1.17. ECAD Zuken CR5000 PWS
 - ① **Zuken CR5000 PWS:** Set the default reading parameters for Zuken CR5000 PWS.

🔝 Environment				×	
General New	Zuken - CR5000 PWS				
Initial View Status					/*/
Layer Stack	Convert EUC-JP to Shift JIS				/* ART_LAY_SPEC (
⊡Tool					*/ /* lavprior color conterpaint surface paint "comments" tone: */
Picking	Layer Set-Up				r)
PCB Explorer	3 Top / Bottom Layer	700	0.077.014		*/ /**********************************
Component Arrangement Plan		TOP	BOLLOM		
ECAD	Silk Screen				ART_LAY_SPEC (1:100:00 THIN: :OFF:OFF:"component hole/square hole":
Altium PCAD	Assy's / Silk-2				2.100:44/THIN :OFF:OFF:" 3.100:11:CONTOUR:OFF:OFF:"TopSiLK";
	Solder Mask				4.100.11.CONTOUR ON OFF-component side test. 5.100.55.CONTOUR OFF-OFF-BotSILK*
CADVANCE	Metal Mask				8:100:22:CONTOUR:OFF:OFF:"component side screen mask"; 8:100:22:CONTOUR:OFF:OFF:"component side solder resister";
- MentorGraphics - Xpedition	Paste Mask				9:100:55:CONTOUR:OFF:OFF:"component side pattern"; 10:100:33:THIN::OFF:OFF:";
MentorGraphics - PADS (*.asc) ODB++	Board Hole				11.100.33.THIN _OFF.OFF."CB Layout Dimension"; 12.100.00.THIN _OFF.OFF."Component side marking drawing"; 13.100.44.CONTOUR:OFF.OFF."component side marking drawing"; 4.100.00.THIN _OFF.OFF.Component side ted drawing";
Zuken - CR5000 Board Designer	Board Contour Laver				15:100:00:THIN :OFF:OFF:'solder side marking drawing'; 16:100:00:THIN :OFF:OFF:'solder side text drawing';
Gerber	To case of using other board	laver specified in BSE			17:100:00.THIN ::OFF:OFF:"; 18:100:22:CONTOUR:OFF:OFF:";
Analysis	i incluse of using other board	ayer speaned in bor			19:100:00:THIN : OFF: OFF: ";
Metal Mask Manager	Board Contour Layer Number				20.100.00.CONTOUR.OFF.OFF
Block Design Generator					22:100.11.THIN :OFF:OFF:";
F-DFM / DFE / DFE+ / DFA	5 Exclude Layers				23.100.44.THIN SUPPOPP."; 24.100.22.CONTOUR.OFF:OFF:"solder side pattern";
DFM					25:100:33:CONTOUR:ON:OFF: solder side solder resister;
DFE					
DFE+	-				
DFA					
Manufacture					
Component Mounting Emulator					
< >					
Save Load			OK Can	cel	

- ② **Encoding**: while reading Japanese ASCII file, user can change EUC JP codes to Shift JIS before design data reading.
- ③ **Layer Setup**: Use this setting to read layer definitions into PollEx PCB design. Zuken PWS designs may have different layer settings depending on users and depending on manufacturing process. To complete this task, refer the BSF(Board Specification File) file used in PWS.
- ④ **Board Contour Layer**: Specify the board contour layer name, in case of using board contour layer differently than that is used in BSF.
- 5 **Exclude Layers**: Exclude specified layers.



1.18. ECAD - Gerber

① **Gerber**: Set the default reading parameters for GERBER file.

😥 Environment		×
General View Layer Layer	Gerber	
Layer Stack	© mm C ir	nch
	A Significant Digit	
PCB Explorer	Diait	3
ECAD	Decimal Point	3
Altium PCAD Altium Designer Cadence - Allegro Expansion CADVANCE MentorGraphics - Board Station, Neutr MentorGraphics - Xpedition MentorGraphics - PADS (*.asc) ODB++ Zuken - CR5000 Board Designer Zuken - CR5000 PWS Gerber 1 Analysis Metal Mask Manager		
Block Design Generator DFM / DFE / DFE + / DFA DFM DFM DFE DFE DFE		
Component Mounting Emulator Component Mounting Security S	v	
Save Load		OK Cancel

- ② **UNIT**: Set the unit of GERBER file.
- ③ Significant Digit: Set the decimal point and effective number of characters for numbers. DIGIT means real part of number and DECIMAL means parts behind "."(dot). Some of GERBER file's representation would be 00235.567. In this case, DIGIT value would be 5 and DECIMAL would be 3. Generally, PollEx PCB ignores the value of DIGIT.

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- ① **Redmark:** Menu for setting Redmark's environment.
- ② **Default Draw Object**: Can set default line with of drawing object.

🔝 Environment		Х
Tool Picking Picking PCB Explorer Component Arrangement Plan CAD Altium PCAD Altium Designer Cadence - Allegro Expansion	RedMark 2) Default Draw Object Line Width 0.3	
CADVANCE MentorGraphics - Board Station, Neutra MentorGraphics - Xpedition MentorGraphics - PADS (*.asc) OB++ Zuken - CR5000 Board Designer Zuken - CR5000 PWS Gerber		
Analysis Metal Mask Manager Block Design Generator □- DFM / DFE / DFE + / DFA DFM DFE DFE DFE DFE DFA		
Manufacture Component Mounting Emulator Make Board Paneling Red-mark 1 Red-mark Plus Restricted PDBB	v	
Save Load	OK Cancel	



1.20. Red-mark Plus

- ① **Red-mark Plus**: Menu for setting Red-mark Plus environment.
- ② **Default to the Environment File**: Can set default Environment File Path.

20 Environment	×
	Red-mark Plus 2) Default Environment Path to the Environment File Altair WPollEx WPollExRedMarkPlus.rmpeny
Altium PCAD Altium Designer Cadence - Allegro Expansion CADVANCE MentorGraphics - Board Station, Neutra MentorGraphics - Xpedition MentorGraphics - PADS (*.asc) ODB++ Zuken - CR5000 Board Designer Zuken - CR5000 PWS	
Analysis Manalysis	
Component Producing Endiator Make Board Paneling Red-mark Red-mark Save Load	OK Cancel



1.21. Restricted PDBB

① **Restricted PDBB**: Menu for setting Restricted PDBB's environment.

7 Environment		×
⊡- Tool Pidking PCB Explorer Component Arrangement Plan	Restricted PDBB DEB Descriptions	
ECAD Altium PCAD Altium Designer Cadence - Allegro Expansion CADVANCE MentorGraphics - Board Station, Neutra MentorGraphics - Ypedition MentorGraphics - PADS (*.asc) OBB++ Zuken - CR5000 Board Designer Zuken - CR5000 PWS Gerber Analysis Metal Mask Manager Block Design Generator DFM / DFE / DFE + / DFA OFE OFE	Initialize stack-up information Initialize Artwork Layer information Remove Board-Contour Initialize Component Name Initialize Net/Component Property Indude Component Outline Include Solder Mask Include Board Figure Include Board Figure Include Mechanical Objects Include Comp Figure Include Comp F	
OFE+ OFA OFA OFA OFA Off Off	~	OK Cancel

2 Exporting Options

Initialize stack-up information: Reset stack-up information and make it with default value.

Initialize Artwork Layer information: Reset artwork layer information and make it with default value.

Remove Board-Contour: Remove board contour data and make it with basic rectangle geometries.

Initialize Component Name: Remove all part's name information and rename them with string starting "PartXXX". All other footprint, package and device name will be re-arranged. Vias and padstacks name will be re-arranged also.

Initialize Net Name: Remove all nets' name and rename them with string starting "NetXXX". Vias and padstacks name will be re-arranged also.

Initialize Net/Component Property: Remove all properties assigned to net and components (reference designator).

Include Component Outline: Include all component outline of component(Artwork Layer-201: COC Top, 202: COC Bottom).

Include Solder Mask: Include all solder mask layer.

Include Metal Mask: Include all metal mask layers.

Include Board Figure: Include all board figures.

Include Mechanical Objects: Include all mechanical objects.

Include Comp Figure: Include all Component Figure Data.



2. Layer

PollEx PCB has two terms to call layers, artwork and physical layer. Physical layer means the physical stack-up layer whereas artwork layer means layer used in ECAD tools. Especially, PollEx PCB has another order of artwork layer. It means artwork layers in PDB have specific purpose depending on index of layers. Following table show the layer's usages in PollEx PCB.

Detail descriptions are followings,

Lay No	Usage	Comment		
1	Тор			
2	Top Pad			
3	Top Solder Resist			
4	Top Silk	For component's ten		
5	Top Silk Text	For component's top		
6	Top Metal Mask			
7~10	Top reserved			
11	Bottom			
12	Bottom Pad			
13	Bottom Solder Resist			
14	Bottom Silk	For component's bottom		
15	Bottom Silk Text			
16	Bottom Metal Mask			
17~20	Bottom reserved			
21	Board Contour Layer			
22	Drill Layer			
23~80	Board Figure Geometries			
81~200	Inner Layer			
201	Top Component Outline	For component's ten		
201~210	Top reserved	For component's top		
211	Bottom Component Geometries	For component's bottom		
211~220 Bottom reserved		For component's bottom		
221~400	Gerber Layer			
401~450	Top reserved	For Component's top		
451~500	Bottom reserved	For Component's bottom		
551~	Board Figure Geometries			



2.1. Layer

To control or set the layer status, use the menu, **Setting > Layer**. (Shortcut key: *Alt* **+** *L*)

_									 		<u></u>								
2	Color T	Α	E	Р	DP	Туре	Attribute	Name	•	V	Color T	A	E	P	DP	Туре	Attribute	Name	
						N		Background								N		Background	
		1	0	1	7	GROUND	POSI	1				1	0	1	7	GROUND	POSI	1	
		2	0	0	5	N	POSI	padstack top				2	0	0	5	N	POSI	padstack top	
	Г	3	0	0	13	N	POSI	Resist-A			Г	3	0	0	13	N	POSI	Resist-A	
		4	0	0	3	N	POSI	Symbol-A			Г	4	0	0	3	N	POSI	Symbol-A	
		5	0	0	4	N	POSI	Symbol-A-1			Г	5	0	0	4	N	POSI	Symbol-A-1	
		6	0	0	14	N	POSI	MetalMask-A				6	0	0	14	N	POSI	MetalMask-A	
		7	0	0	15	N	POSI	HeightLimit-A				7	0	0	15	N	POSI	HeightLimit-A	
		8	0	0	16	N	POSI	inhibit(plc)-A				8	0	0	16	N	POSI	inhibit(plc)-A	
		9	0	0	17	N	POSI	inhibit(plc)-C				9	0	0	17	N	POSI	inhibit(plc)-C	
		10	0	0	18	N	POSI	inhibit(wir)-A				10	0	0	18	N	POSI	inhibit(wir)-A	
		11	0	6	12	GROUND	POSI	6				11	0	6	12	GROUND	POSI	6	
		12	0	0	10	N	POSI	padstack bottom				12	0	0	10	N	POSI	padstack bottom	
	Γ	13	0	0	19	N	POSI	Resist-B				13	0	0	19	N	POSI	Resist-B	
		14	0	0	8	N	POSI	Symbol-B				14	0	0	8	N	POSI	Symbol-B	
	Г	15	0	0	9	N	POSI	Symbol-B-1				15	0	0	9	N	POSI	Symbol-B-1	
		16	0	0	20	N	POSI	MetalMask-B				16	0	0	20	N	POSI	MetalMask-B	
		17	0	0	21	N	POSI	HeightLimit-B				17	0	0	21	N	POSI	HeightLimit-B	
		18	0	0	22	N	POSI	inhibit(plc)-B				18	0	0	22	N	POSI	inhibit(plc)-B	
		19	0	0	23	N	POSI	inhibit(wir)-B				19	0	0	23	N	POSI	inhibit(wir)-B	
		21	0	0	1	N	POSI	BOARD_FIGURE			Г	21	0	0	1	N	POSI	BOARD_FIGURE	
		22	0	0	2	N	POSI	HOLE				22	0	0	2	N	POSI	HOLE	
		23	0	0	28	N	POSI	mark				23	0	0	28	N	POSI	mark	
		24	0	0	29	N	POSI	Free1	•			24	0	0	29	N	POSI	Free1	
	per									1									

- ① **Artwork Layer**: Select this button to show layer orders with artwork layers.
- 2 **Physical Layer**: Select this button to show layer orders with physical layers.
- ③ Each column's abbreviation means properties of layers.
 - **V**: Make visible On/Off for layer.
 - **T**: Make transparent layer status.
 - A: PollEx PCB's artwork layer number.
 - E: ECAD artwork layer number.
 - **P**: Physical layer number.

DP: Display Priority for showing layer. Lower number layer will be displayed at top.

Type: Physical layers' type.

Attr: Layer attributes. Values will be one of positive or negative

Name: Layer name.

With layer control window, user can do work for selecting layer, making layer status visible/invisible.



- ④ At layer type selection, select one between artwork and physical layer.
- 5 Among layer list, select one of layers.
- 6 Launch **Layer** window for detail set-up for layer status.



3. Measure

Measure tool is a function to measure the size or dimension of objects. Use the menu, **Setting > Measure**.



After launching measure tool, user can see above dialog window at right sides in main window.

- ① Select measuring type and object to measure.
- ② Measuring results will be displayed at property window. Text displaying ratio on screen is set as 100%. However, user can change the text scale if the showing text size is small and user wants to increase the size. **Keep** button maintain this ratio until the window is closed.

Upon using following proper function, user can easily check the size or distance between objects.

- Point to Point: Measure the distance between two points.
 - Line, Arc: Measure line or arc's segment length.
 - Route Length: Measure total net length.



- **Route Segment Length**: Measure selected segment length in routing net.
- Comp to Comp Dist: Measure center to center for components.
- **Pad(Via) to Via(Pad)**: Measure pad(via) to another pad(via).
- Object to Object: Measure object to object.

4. Picking

This is the tool for checking the properties of certain objects on board by mouse picking. Use the menu, **Setting > Picking**.



After launching picking tool, **Picking Tool** dialog box will be shown at right-side on the screen. Upon selecting object(①), selected objects properties or information will be shown on tab(⑥and⑦) window. Especially, at tab window ⑥, PollEx PCB shows board's hierarchical structure for selected objects. At window tab ⑦, all related object's properties will be shown. Followings are each tab's name and usages.

- ① Picked object on screen.
- ② **Filter**: Filter for selecting target objects.
- ③ Selection either All or Segment for routing net.
- ④ **Neighborhood Object**: Select object in given area for routing net or component.
- **5 Picking Layer**: Select layers which users want to select. Default is all layers.
- 6 Selected object listing window.
- ⑦ Property tab to show selected objects' properties.



5. Unit Conversion

Basically, PollEx PCB uses the unit from ECAD design. But user can change the unit of design. To do this, use the menu, **Setting > Unit Conversion**.

🔀 Unit Conversion	×
Current Unit	MM X 10 0
Unit Selection • mm • Inch	C Mil C Micro Meter
User Define Unit	Selected Unit X 10 ^ 0
Change Unit	Cancel

PollEx PCB supports 4 different units, mm, Inch, Mil and Micrometer. Select target unit and press **Change Unit** button to complete changing unit.



6. Board Information

Board Information menu shows all information for design. Use the menu, **Setting > Board Information**.

🛛 🖉 👯 间	
Board Information	×
File Information	
Import File Version	2.1
CAD File Create Date	Tue Apr 03 17:23:57 2018
CAD File Path	
C: WTempWAltar-PollEx	CWPCBWPollEx_New_Samp
	PollEx New Sample-rev0
Comment	
PCB Information	
Unit	MM
Library Padstack Quantity	36
Part Library Quantity	42
Working Size	63.60 X 11268.71
PCB Size	63.60 X 65.40
Number of Physical Layer	6
Reference Quantity	
Placed Reference Quant	ity 282
	antity j U
Net Quantity	
Routed Net Quantity	217
Unrouted Net Quantity	0
Placed Pin Quantity	1268
Export to Excel	Close

User can check the board creation date, file path, unit, board size, number of components on board, number of nets, and other information.



View

User can use **View** menu to control display more efficiently.

	View	Properties	Tools	Analysis
		Previous	Ctrl	+ Z
		<u>N</u> ext	Ctrl	+ Y
	A	Zoom <u>I</u> n -	+, pull w	heel
	Q	Zoom <u>O</u> ut -,	push w	heel
1	Q	Zoom <u>W</u> indow	Alt	+ W
		Zoo <u>m</u> 1:1	Alt	+ 1
		Toggle 1:1	Ctrl +	Tab
2	Í	Set Capture W	/indow	
ি		Mirror View	Ctrl	+ M
9		Board Rotation	r.	•
	•	Route On/Off		
		Component Or	n/Off	
4	(Polygon <u>F</u> ill		
		Display Setup		
		Net Display On	/Off	
(5)		Board Mini-map)	
	<	<u>M</u> enubar		
6	~	Toolbar		
	~	<u>S</u> tatus Bar		

- ① Zoom In/Out/Window/Zoom 1:1 Toggle 1:1: use the menu to control view status.
- ② Set Capture Window: Screen capture option.
- ③ Mirror View/Board Rotation: make mirror for board's image or rotate board.
- ④ Route/Component On/Off, Polygon Fill/Unfill, Net Display On/Off: control the objects' viewing status on board.
- (5) Board Mini-Map: show small map with which user can see whole board and working area.
- 6 Bar Menus.

1. Set Capture Window

Use this function to make partial image capture, screen capture, full area capture. Saved image will be saved in system buffer for using other Windows applications. Use the menu, **View > Set Capture Window**.





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Fix the screen and press the above menu button. Next, select two points on screen with mouse click to set rectangle area. Then pressing the key **Ctrl + C** will save image into system buffer. To use system buffer image, use the key **Ctrl + V**.



2. Mirror View / Board Rotation

User can see the mirrored board image with **Mirror View** menu. Also, user can see the rotated board using **Board Rotation** menu.

2.1. Mirror View

Use the menu, **View > Mirror View**. Many cases, user needs to see the bottom shape with mirrored status to compare to real PCB image.





2.2. Board Rotation

Use the menu, **View > Board Rotation**. PollEx PCB supports rotation angles for 90, 180, 270 and user defined angle.

Original
90
180
270
User Defined



3. Route on, off / Component on, off / Polygon Fill, Unfill

To see components, routing pattern and copper pour more efficiently, use these menus. All below three menus are running with toggle mode.

View > Route On/Off

- View > Component On/Off
- View > Polygon Fill/Unfill









4. Net Display On/Off

PollEx PCB can display or turn off display for a certain net(s). Use the menu, **View > Net Display On/Off**.



- ① Checking "V" column turn on and off for selected nets.
- ② After selecting nets, pressing **OK** button will apply changes to screen.

5. Board Mini-Map

While exploring PCB design, this function help user to check current location regarding to whole board and see the whole board image. Using the following menu to launch the min-map window, **View > Board Mini-Map**.



On mini-map, red line means the board contour.



6. Menubar, Toolbar, Status bar

Menubar contains main menu list and tool bar contains icon menus and status bar show working status, respectively. User can hide each menu using following menus.

View > Menu bar



Properties

Properties menu has 5 different sub menus, **Nets**, **Composite Nets**, **Parts**, **Material Library** and **Layer Stack**. Using sub-menus, users can see and edit properties of objects on board or library link.

<u>P</u> ro	perties	<u>T</u> ools	<u>A</u> nalysis			
	Nets					
	Compo	site Net	s			
	Net Cla	sses				
	Net Bu	ses/Groups				
	Parts					
	Compo	nents				
	Materia	l Library				
	Layer S	Stack				
	Rigid-Fl	exible P(в			

1. Nets

Net's properties are basic attributes influencing the electrical analysis. The voltages assigned to the Power/Ground net will be applied to the connected terminator pin as termination voltage. Net pairs defined as **Differential Signal Positive (+) & Negative (-)** will be recognized and simulated as differential pair by just assigning the driver model to one of both Positive (+) or Negative (-) net. **Properties - Nets** menu will invoke a dialog with default net properties as **Single-ended signal** for all nets included in the activated PCB system, by double clicking a net or selecting a net and clicking the **Edit** button, user can define or modify the **Net Type**(2), **Voltage**(5) and electrical constraints(1). By

clicking the *Pin list*(6), user can verify the list of all pins connected to the selected net.

Basic Electrical Constraints								N P
Net Name	Net Type ②	Net Class	Differential Pair Net 3	Composite Net		Voltage (V) 5	Pin List 6	Í
5VCC	Power	Power V	Vhen a termin	ator pin is co	nnected to a	5	Pin list	
VCC1P5_DDR	Power	Power P	ower of grou	nd net, the ter	mination	1.5	Pin list	
VCC1P8_ADC_REF	Power	Power fr	oltage will be	automatically	assigned	0.75	Pin list	
VCC_DDR_REF	Power	Power g	round net.	ge applied to	the power of	0.75	Pin list	
VCC_MCU_AREF	Power	Power				0.75	Pin list	
SIGN00376	Single-ended signal			CN- MCU_SDA_	0 SIGN00376 9	0	Pin list	
SIGN00377	Single-ended signal			CN- MCU_SCL_:	L SIGN00377	0	Pin list	
SIGN00378	Single-ended signal			CN- MCU_SDA_	1 SIGN00378	0	Pin list	
MCU_PADQS0	Diff Signal -	DDR_DQS	MCU_NADQS0			0	Pin list	
SIGN00379	Single-ended signal			CN- MCU_SCL_2	2 SIGN00379	0	Pin list	
MCU_HDMI_TX0N	Diff Signal -	DDR_DQS	MCU_NADQS1			0	Pin list	
MCU_PADQS2	Diff Signal -	DDR_DQS	MCU_NADQS2			0	Pin list	
VCC2P8_GMAC	Power	Power				0	Pin list	
MCU_PADQS3	Diff Signal -	DDR_DQS	MCU_NADQS3			0	Pin list	
SDA_5V	Single-ended signal	Power				0	Pin list	
MCU_ANCAS	Single-ended signal	DDR_Comma	n			0	Pin list	
VCC1P0_ALIVE	Power	Power				0	Pin list	
MCU_D20	Single-ended signal	DDR_Data				0	Pin list	
MOL DOI	Cinals and ad sizes!	DDD Data				0	na ha	1



By clicking the **Assign Net Type**, user can set net property automatically using net information which described in IBIS files and property.

By clicking the *Find Net Class*, user can set net class automatically using pre-defined net class search string file.

2. Composite-nets

When two or more nets are serially connected through passive components such as resistor, electrical analysis must be made for the entire signal path encompassing the multiple nets connected with these passive components. These nets are modeled as composite nets in PollEx PCB environment. The composite nets are automatically generated by PollEx PCB which references the schematic data to configure it by checking the connectivity of the selected passive components to each net.



In the upper left figure, two nets are connected with the **R207** resistor, without composite nets operation, these two nets might have **open** terminal for each then electrical simulation results for the nets wouldn't be appropriate.

Properties - Composite Nets menu provides versatile ways to manipulate the **Composite Nets** generation and manage features with many options and operations illustrated below.



Altair PollEx 2021 User Guide

РСВ

1 🔽 Resistor 🔽 Capacitor	Inductor	Conter Passive				
Basic Electrical Constraints		7.99 N. N.				4 ⊅
et Name	Net Type	Net Class	Differential Pair	Composite Data	Pin List 🕧	
I- MCU_HDMI_TX0P SIGN00249	Composite Diff+	None		Composite Data	Pin list	
- MCU_HDMI_TX1N SIGN00251	Composite Diff-	None		Composite Data	Pin list	
_						
8						

In **Composite Component Area** (1), user can select components to be used to generate composite net. Two nets connected with this component are modeled as composite nets.

After selecting composite component, upon clicking *Generate Composite Nets* 10 button, the list of composite nets will be displayed on **composite net result display region** 8.

User can remove or edit composite net result by **Remove** or **Edit** button.

By double clicking one of composite net, the Edit dialog will be displayed. User can change **Net Type**, **Net Class** and **Electrical Constraints**.

Net energy	Net Clean	
Net name	Net Class	
CN-IMCU_HDMI_TX0P[[SIGN00249]]	None	•
Net type		
Composite single	_	
Differential pair		
	v	
ectrical Constraints Max crosstalk jitter (ps)	Operating frequency (MHz)	Eye mask height (V)
Ax crosstalk jitter (ps)	Operating frequency (MHz) 500 Max differential pair skew (os)	Eye mask height (V) Default Default Eve mask top/bottom width (%)
ectrical Constraints Max crosstalk jitter (ps) 100 Max near-end crosstalk noise (V) 0.15	Operating frequency (MHz) 500 Max differential pair skew (ps) 100	Eye mask height (V) Default Default Eye mask top/bottom width (%)
Actrical Constraints Max crosstalk jitter (ps) Max near-end crosstalk noise (V) 0.15 Max far-end crosstalk noise (V)	Operating frequency (MHz) 500 Max differential pair skew (ps) 100	Eye mask height (V) Default Default Eye mask top/bottom width (%) Grant and the mask middle width (%)
A crosstalk jitter (ps) Max crosstalk jitter (ps) Max near-end crosstalk noise (V) Max far-end crosstalk noise (V) 0.15	Operating frequency (MHz) 500 Max differential pair skew (ps) 100	Eye mask height (V) Default Default Eye mask top/bottom width (%) Seye mask middle width (%) S
A crosstalk jitter (ps) Max crosstalk jitter (ps) Max near-end crosstalk noise (V) 0.15 Max far-end crosstalk noise (V) 0.15	Operating frequency (MHz) 500 Max differential pair skew (ps) 100	Eye mask height (V) Default Default Eye mask top/bottom width (%) Several mask middle width (%)





By clicking **Pin List** field, user can review the component and pin number connected to this composite net.

Component	Pin Name	Pin Type
U1	B24	IO
R90	1	IO
R90	2	IO
CN1	7	IO

3. Net Classes

User can classify nets according to their electrical characteristics. By using net class assigned to each net, DDR nets are automatically grouped when performing **Automatic DDR Bus Analysis**.

Upon selecting **Properties-Net Classes** menu, a default net class, string filter, is displayed as shown below.



РСВ

Net Classes		×
	String search def	finition
Class Name	Search Strings	^
DDR_DQS	[*DQS*]	
DDR_Data	[*_D#*]	
DDR_DM	[*_DQM#*]	
DDR_CLK	[*_CLK*],[*_ACK],[*_ACKB]	
DDR_Address	[*_A#*],[*_AA#*]	
DDR_Command	[*_BA#*],[*_ABA#*],[*RAS*],[*CAS*],[*_WE*],[*_ANWE*]	
DDR_Control	[*_CS#*],[*_ACS#*],[*_CKE*],[*_ACKE*],[*ODT*]	
Power	[*VCC*],[*#V],[*REF*],[*#.#V*]	
Ground	[*GND*]	
HDMI_Clk	[[*HDMI*]&[*TXC*]]	
HDMI_Data	[[*HDMI*]&[*TX#*]],[[*HDMI*]&[*TX#?]]	
LVDS_Clk	[[*LVDS*]&[*CLK*]]	
LVDS_Data	[[*LVDS*]~[*CLK*]]	
SATA_Tx	[[*SATA*]&[*TX*]]	
SATA_Rx	[[*SATA*]&[*RX*]]	
USB2	[[*USB*]&[[*+][*-][*P][*N][*M]]],[*USB*-],[*USB*+]	
USB3_Tx	[[*USB3*]&[*TX*]]	
USB3_Rx	[[*USB3*]&[*RX*]]	
CSI_Clk	[[*CSI*]&[*CLK*]]	
CSI_Data	[[*CSI*]~[*CLK*]]	
DSI_Clk	[[*DSI*]&[*CLK*]]	
DSI_Data	[[*DSI*]~[*CLK*]]	
PCIe_Tx	[[*PCIe*]&[*TX*]]	
DCTA RV	[[*DCI_*]&[*QY*]]	*
Import	Export Add Edit Remove OK Ca	ancel

User save and re-load net class file using **Import** and **Export** button. User can edit current net class item using **EDIT** button, add a new net class item using **Add** button.

Upon clicking *Add* button, the **Net Classes** dialog will be open. User can assign new **net class name** and **search strings**. Two operators are used in the search string: # and *.

*: Any string

#: One Number

This net class definition will be used at **Properties-Nets** menu to assign net class to each net. By using net class assigned to each net, DDR nets are automatically grouped when performing **Automatic DDR Bus Analysis**.

4. Net Buses/Groups

User can generate Net Group or Bus Group using this menu. This will be used for PollEx DFE+ option. User can classify nets according to their electrical characteristics. By using net class assigned to each net, DDR nets are automatically grouped when performing **Automatic DDR Bus Analysis**.

Upon selecting **Properties-Net Buses/Groups** menu, the Net Buses/Groups dialog will be open. Just clicking **Generate DDR Buses** button, the DDR Bus groups will be generated automatically. In this process, it creates a following table by referring to **Net Classes** and **Electrical constraints** of nets.

User can add arbitrary bus group using **Add** button.

РСВ

Net Buses/Groups	;				X
Bus/Group Name	Max Bus Skew (ps)	Max Strobed Skew (ps)	Strobe Net	Control Device	Net Names
DDR_Data_B0	50	5	0 MCU_NADQS0, MCU_PADQS0	U1	MCU_D0, MCU_D1, MCU_D2, MCU_D3, MCU_D4, MCU_D5, MCU_D6, MCU_D7, MCU_DQM0
DDR_Data_B1	50	5	0 MCU_NADQS1, MCU_PADQS1	U1	MCU_D8, MCU_D9, MCU_D10, MCU_D11, MCU_D12, MCU_D13, MCU_D14, MCU_D15, MCU_DQM1
DDR_Data_B2	50	5	0 MCU_NADQS2, MCU_PADQS2	U1	MCU_D16, MCU_D17, MCU_D18, MCU_D19, MCU_D20, MCU_D21, MCU_D22, MCU_D23, MCU_DQM2
DDR_Data_B3	50	5	0 MCU_NADQS3, MCU_PADQS3	U1	MCU_D24, MCU_D25, MCU_D26, MCU_D27, MCU_D28, MCU_D29, MCU_D30, MCU_D31, MCU_DQM3
DDR_Address	50	5	0 MCU_ACK, MCU_ACKB	U1	MCU_AA0, MCU_AA1, MCU_AA2, MCU_AA3, MCU_AA4, MCU_AA5, MCU_AA6, MCU_AA7, MCU_AA8, MCU_AA5
DDR_Command	50	5	0 MCU_ACK, MCU_ACKB	U1	MCU_ABA0, MCU_ABA1, MCU_ABA2, MCU_ANCAS, MCU_ANRAS, MCU_ANWE
DDR_Control	50	5	0 MCU_ACK, MCU_ACKB	U1	MCU_AODT0, MCU_ACKE0, MCU_ACS0
Generate DDR I	Buses	Add	Remove Edit		OK Cancel

5. Parts

Show the parts information. Use the menu, **Properties > Parts**.

Parts menu show the status of the properties assignment to the parts which are included in the current PCB system to analyze. The unified parts created by PollEx UPE (Unified Part Editor) can have versatile information such as electrical buffer model, package thermal parameters and 3D package geometry which needed for electrical, thermal and 2D/3D assembly analysis (by **PollEx DFA** and **PCB assembly viewer**) and it would be stored in specific folders in local or server system.

Parts												Х
Part Name (CPN) A	UPF Name (MPN)		Footprint	Package	Functional Type	Passive Value	Pin Count	Package	Electrical	Thermal	Refere	^
AB38T-32.768KHZ	AB38T-32.768KHZ	•	XT-32.768	XT-32.768	Other		2	- Č			X102	
ASFL1-16MHZ	ASFL1-16MHZ	Ŧ	XTAL-ISC32	XTAL-ISC32	Other		4	(X101	
BOOT_MODE	BOOT_MODE	Ŧ	PAD2P-1.0X1.0	PAD2P-1.0X1.0	Other		2	(Т3	
BSS123	BSS123	•	SOT23	SOT23	Discrete		3	(Q1,Q2	
CIC05P121NC	CIC05P121NC	•	FB1005-3PCB	FB1005	Inductor	Variable	2	(FB3,FB	
CIM05F750NC	CIM05F750NC	•	RES1005	RES1005	Inductor	Variable	2	(FL1,FL	
CL05C150JB5NNNI	CL05C150JB5NNND	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C103,0	
CL05C270JB5NNW	CL05C270JB5NNWC	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C116	
CL05F103ZB5NNN	CL05F103ZB5NNNC	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C109,(
CL05X105MR3LNN	CL05X105MR3LNNH	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C220,(
CL10Y106MQ8NRM	CL10Y106MQ8NRNC	•	CL1608-5PCB	CL1608	Capacitor	Variable	2	(C85,C8	
CLL5Y104MQ3NLN	CLL5Y104MQ3NLNC	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C82,CE	
ERJ6GEYJ101	ERJ6GEYJ101	•	R-CHP-2125-F	R-CHP-2125	Resistor	Variable	2	(R226,F	
H5TQ4G63AFR	H5TQ4G63AFR	•	IC-BGA96/K4B4G1	IC-BGA96/K4B4G1	Digital IC	H5TQ4G	96	(U204,I	
IC-NXP4330	IC-NXP4330	•	IC-BGA-513P	IC-NXP4330	Digital IC	NXP4330	513	(U1	
RC1005F241CS	RC1005F241CS	Ŧ	R1005-2PCB	R1005	Resistor	Variable	2	(R231,F	
RC1005J000CS	RC1005J000CS	•	R1005-2PCB	R1005	Resistor	Variable	2	(R1,R1(~
<											>	
Link												a
Part library director	C:WIempWAltair-Pol	IEX	WPOIEX_RadiatedEmi	SSION WUPPS								
MPN Reference file	C:₩Users₩eunkyou	ngʻ	₩AppData₩Roaming	₩Altair₩PollEx₩Data	WMPN_Reference.:	xls]
Synchronize	Export MS Excel Edit I	MPI	N Reference	Edit Elec/Therm	al Prop Edit Pa	ickage Geo	m Fi	nd by Ref De	esignator	Clos	e	

6. Components

Components menu lists all components (reference designators or location identifiers) in current design. In this menu users can assign different RLC value to each different



Upon double clicking the passive component, the **Set Passive Data** dialog will be open.

Set Passive Data			×
Passive Type			
Resistor			-
Resistance (Ohm)			
100			
	ОК	Ca	ancel

Then user can select **Passive Type** and enter the **Resistance**.

Upon clicking *Find Passive Component Value* button, user can assign all the passive component's **Type** and **Value** automatically.

Basic										
Ref Designator	Part Name (CPN)	UPF Name (MPN)	Footprint	Placed Layer	x	Y	Rotation	Passive Type ∇	Passive Value	
R19	RC1005J000CS	RC1005J000CS	R1005-2PCB	тор	20.400	-6.700	90	Resistor	00hm	
R20	RC1005J103CS	RC1005J103CS	R1005-2PCB	тор	19.300	-6.700	90	Resistor	10MOhm	
R21	RC1005J103CS	RC1005J103CS	R1005-2PCB	тор	23.700	-3.000	90	Resistor	10MOhm	
R22	RC1005J000CS	RC1005J000CS	R1005-2PCB	ТОР	24.800	-3.000	90	Resistor	00hm	
R23	RC1005J000CS	RC1005J000CS	R1005-2PCB	ТОР	24.300	-6.500	90	Resistor	00hm	
R24	RC1005J103CS	RC1005J103CS	R1005-2PCB	тор	25.400	-6.500	90	Resistor	10MOhm	
R25	RC1005J000CS	RC1005J000CS	R1005-2PCB	тор	19.300	-9.400	270	Resistor	00hm	
R26	RC1005J103CS	RC1005J103CS	R1005-2PCB	тор	18.300	-6.700	90	Resistor	10MOhm	
R27	RC1005J000CS	RC1005J000CS	R1005-2PCB	тор	18.300	-9.400	270	Resistor	00hm	
R28	RC1005J103CS	RC1005J103CS	R1005-2PCB	тор	20.300	-9.400	270	Resistor	10MOhm	
R29	RC1005J103CS	RC1005J103CS	R1005-2PCB	ТОР	22.200	-9.300	90	Resistor	10MOhm	
R30	RC1005J000CS	RC1005J000CS	R1005-2PCB	тор	23.300	-9.300	90	Resistor	00hm	
R31	RC1005J000CS	RC1005J000CS	R1005-2PCB	тор	26.500	-6.500	90	Resistor	00hm	
R32	RC1005J103CS	RC1005J103CS	R1005-2PCB	ТОР	27.600	-6.500	90	Resistor	10MOhm	
R33	RC1005J103CS	RC1005J103CS	R1005-2PCB	BOTTOM	13.780	-6.110	180	Resistor	10MOhm	
R34	RC1005J103CS	RC1005J103CS	R1005-2PCB	BOTTOM	11.570	-5.395	0	Resistor	10MOhm	
R35	RC1005J103CS	RC1005J103CS	R1005-2PCB	BOTTOM	16.153	-7.410	180	Resistor	10MOhm	
R36	RC1005J515CS	RC1005J515CS	R1005-2PCB	ТОР	1.500	-18.310	180	Resistor	5.1TOhm	
500	DC100E110ECC	DC100E110ECC	DIONE ODCD	TOD	4 600	4 000	100	Desistor	1 TOhm	

7. Material Library

Material Library menu lists materials library which could be used in PCB manufacturing. PollEx PCB supports default library list, but user can add new material or edit them. This material's properties can be used in **Signal Integrity** or **PCB Thermal** analysis. Use the menu, **Properties > Material Library**.



РСВ

Materials										×
Name /	Туре	Frequency (MHz)	Dielectric Constant	Loss Tangent	Electric Resistivity (Ohm.m)	Relative Magnetic Permeability	Thermal Conductivity X (W/m.K)	Thermal Conductivity Y (W/m.K)	Thermal Conductivity Z (W/m.K)	1
AIR	Dielectric		0 1	0			0.0265	0.0265	0.0265	
ALLOY42	Conductor		0		6e-07	1	12.5	12.5	12.5	
ALUMINA94%	Dielectric		0 9	0.005			18	18	18	
ALUMINA96%	Dielectric		0 9	0.005			35	35	29.4	
ALUMINIUM-0TMPR	Conductor		0		2.73e-08	1	216.3	216.3	221.8	
ALUMINIUM-6061T6	Conductor		0		2.73e-08	1	155	155	167	
ALUMINIUM-NITRIDE	Dielectric		0 8.3	0.005			170	170	170	
BERYLLIA	Dielectric		0 6.8	0.001			155.71	155.71	155.71	
COPPER	Conductor		0		1.678e-08	1	370	370	394	
FR4	Dielectric		0 4.5	0.02			0.35	0.35	0.35	
GLASS-EPOXY	Dielectric		0 4.3	0.005			0.26	0.26	0.26	
GOLD	Conductor		0		2.25e-08	1	297.2	297.2	297.2	
INVAR	Conductor		0		8.33e-08	1	81.8	81.8	81.8	
KOVAR	Conductor		0		4.9e-07	1	14.2	14.2	14.2	
LEAD	Conductor		0		2.174e-08	1	32.7	32.7	32.7	
MOLYBDENUM	Conductor		0		5.52e-08	1	142.3	142.3	142.3	
MULLITE	Dielectric		0 6.4	0.005			6	6	6	1
NICKEL	Conductor		0		7.16e-08	1	92	92	92	
PLATINUM	Conductor		0		1e-07	1	71.6	71.6	71.6	
POLYIMIDE	Dielectric		0 4.5	0.01			0.26	0.26	0.26	
SILICON	Conductor		0		3160	1	83.7	83.7	83.7	•
Import	Export	Remov	re A	dd Dielectric	Add Conduc	ctor	Edit		OK Cancel	1

Default library file's location is

C:\Users\%USER_NAME%\AppData\Roaming\Altair\PollEx\Data\Default_material.mtrl.

8. Layer Stack

Layer Stack menu shows PCB's physical stack up structure. User can edit each layer's type, material and thickness. User can also import, export, add, remove and insert. This information will be used in **PollEx SI** and **PollEx Thermal** analysis. Use the menu, **Properties > Layer Stack**.

Layer S	itack								×
Layer	r Stack								4 ⊳
No.	Name	Туре	Thickness (mm)	Conductor Materia	Dielectric Material	Color	Trace Width Wider Etching Difference Trace Side (mm)	_	
1	1	Ground -	0.035	COPPER -	AIR 🔻	-	0 ВОТТОМ 🔻		-
	Dielectric Layer	Dielectric 🔻	0.065	-	FR4 💌	-	0 ВОТТОМ 🔻		
2	2	Ground 🗸	0.035	COPPER -	FR4 💌	-	0 BOTTOM -		
	Dielectric Layer	Dielectric -	0.15	-	FR4 -	-	0 BOTTOM 👻		
3	3	Ground -	0.035	COPPER -	FR4 -	-	0 BOTTOM -		
	Dielectric Layer	Dielectric 🔻	0.15	-	FR4 🔻		0 BOTTOM 🔻		•
4	4	Ground -	0.035	COPPER -	FR4 🔻	-	0 BOTTOM -		
	Dielectric Layer	Dielectric 🔻	0.15	-	FR4 🔻		0 BOTTOM 🔻		
5	5	Power -	0.035	COPPER -	FR4 💌	-	0 BOTTOM -		-
	Dielectric Layer	Dielectric -	0.065	-	FR4 -	-	0 BOTTOM 🔻		
6	6	Ground -	0.035	COPPER -	AIR 👻	-	0 BOTTOM -		
								Total thickness (mm)).79
1	Import Export	Add	Re	move Ir	nsert Export	MS Excel	Apply	OK Cance	4

9. Rigid-Flexible PCB

Define the flexible area of the rigid-flexible PCB.



_____p.99

PCB

aver det	PCB Area	ible area						1
Min X	Min Y	Max X	Max Y	Top Signal Layer	Bottom Signal Layer	Coverlay Material	Top Coverlay Thickness	Bottom Coverlay Thickness
					Layer		Thickness	Thicknes
	2 Add				3 Edit		4	Remove
					_			
_								

① Layer defining flexible area: Designate the artwork layer (NOT physical layer) that is set as the flexible area

Find the objects in the layer and automatically record them in the table.

② Add: Settings for the flexible (bending) area on the Rigid-flexible PCB design

Flexible PCB Areas
Flexible Area
Min X 0 Max X 0 Select
Min Y 0 Max Y 0
Layer
Top Signal Layer
Bottom Signal Layer
Coverlay
Coverlay Material
Top Coverlay Thickness 0
Bottom Coverlay Thickness 0
OK Cancel

- Flexible PCB Area: Set the layer where the bending area is designed, or the user sets the area.



- Layer: The flexible layer is defined as the starting and ending layers of the physical layer.
- Coverlay: Set the Coverlay property information.
- $\ensuremath{\textcircled{}}$ Bdit: Modify the saved settings.
- $\textcircled{\sc d}$ Remove: Delete the saved settings from the lists.
- $\ensuremath{\mathbb{5}}$ $\ensuremath{\,}$ Press the OK button to save the settings.

Tools

Under **Tools** menu, there are many useful functions. Almost functions help users to get documents or reports for nets or components.



- 17 Compare GDSII
- ① PCB Explorer
- 2 Change Reference Names
- ③ Change Board Origin
- ④ Go to Location
- **5** Component Arrangement Plan
- 6 PCB Data Extractor
- ⑦ Extract Decap Data
- 8 Net Color
- 9 Net Length View
- 10 Net Analyzer
- 1) Change Net Name
- ① Thermal Resistance Calculator
- 13 Gerber Transformation
- I Visual Layer Composition
- 15 BOM Changer
- 16 Worksheet Planner
- 17 Golden Sample
- 18 Compare GDSII

1. PCB Explorer

PCB Explorer helps user to search components or nets. Also, it provides searching objects of combination for net and net connected components or component and connected nets. Use the menu, **Tools > PCB Explorer**.



РСВ

PCB Explorer	×
Selection Type - A	
Search (3)	Search
4 Part C R	ef C Net
47151-0001 675031020 AB38T-32.768KHZ ASFL1-16MHZ BOOT_MODE BS5123 CIC05F121NC CL05F1032B5NNNC CL05F1032B5NNNC CL05C1503B5NNND CL05C2703B5NNNUC CL05C2703B5NNNUC	
	▼ I Sud Dim
Clear Color	Exc Disp
	Contrast
	© And
None C Part C Re	f C Net

- ① Selection Type A: Basic search window (Type-A).
- ② Selection Type B: Second search window (Type-B).
- ③ Searching keyword input box. If user wants to search the Part, Reference or Net name, use this. Also, users can search keyword input box with Wild Card(*, ?, #) in PCB Explorer. Search keyword is case-insensitive.
 - *: String
 - ?: One Character
 - #: One Number

" ": Searching the matching string only.

④ Objects selection in the basic search window.

Example 1) Search String: c1

Search Result: *C1, C10, C11, IC1, IC10, IC11 etc.

Example 2) Search String: gr red blu Search Result: GREEN, GREEN1, RED, RED1, BLUE, BLUE1 etc.

Example 3) Search String: "green" "red" "blue" Search Result: GREEN, RED, BLUE

Example 4) Search String: 1* Search Result: 1S335-BP, 1SV164 etc.

Example 5) Search String: *1* Search Result: 1S335-BP, 1SV164, AD724JR-16-IC, ERJ6GEYJ101, ERJ6GEYJ301, ERJ6GEYJ331 etc.



	Example 6) Search String: ?#1# Search Result: C210, C211, C212, R214, U210 etc.
	Example 7) Search String: ?c5 Search Result: *C5, IC5 etc.
	Example 8) Search String: "c6"" Search Result: C6"
Inc No	cluding Wild Card(*, ?, #) in string, enter " ' " ahead of the Wild Card. t including Wild Card(*, ?, #) in string, " ' " is regarded as the character. Example 1) Search String: CLK'* Search Result: CLK*
	Example 2) Search String: CLK'A Search Result: CLK'A
5	 View control buttons on screen. Clear: reset selection. Color: assign color for selected objects. Excl: display only selected objects. For others, PollEx PCB will not show them. Disp: make high-light for selected objects. Contrast: display unselected objects with gray color.
6	Combination methods selection for objects on basic window and second window.

⑦ Second window's object selection.

Basically, PollEx PCB Explorer runs with two windows, ① and ②. If user wants to search certain objects on PCB, using **Selection Type-A** would be enough. However, if user wants to find a certain net and connected components for selected net, use **Selection Type-B**. In this case, select with **Net** in the **Selection Type – A** and Ref in the **Selection Type – B**.



2. Change Reference Names

If user wants to change the reference name, use this function. But, once reference name is changed, inner data structure is also changed. So be cautious to use this function. Use the menu, **Tools > Change Reference Names**.



- 1 Select reference which user wants to change reference name.
- ② Give target string to be changed and press action button among Change, Add Prefix or Add Suffix.



③ Press **Save/Upload** button change and save for update.

3. Change Board Origin

If the origin point of PCB design is incorrect, user can change its origin point with this function. Use the menu **Tools > Change Board Origin**.



- ① Origin and left bottom of board outline are away. If checking Set Origin to Let Bottom button, move origin based on left bottom of board outline. At this time, difference is calculated, it can see values in X, Y-Coordinate.
- ② Object Select: Select the object to be origin.
- ③ After specifying new origin point, pressing **Save/Upload** button will change the origin point of board.
- ④ To go back to initial status, use the button, **Initialize Board Origin**.



If user moves mouse cursor to certain point, use this function. Use the menu, **Tools > Go to Location** (Shortcut key: Alt + G).



Ready

x: -12.99 y: 20.89

- ① Give the target location to which user wants to move mouse cursor.
- ② Also, at this column, user can give location from paste function from other application.
- ③ If checking **Auto Zoom In**, give the target location with auto zoom-in.
- ④ Setting two locations will zoom in screen with rectangle area with given two points.
- 5 **Apply** button will do action.

To input location with manually, x and y locations should be separated with ","(comma). After Apply action, searched location will remain with "+" mark until the window is closed.



5. Component Arrangement Plan

This function gives user to replace paper type worksheet into report. This function shows on-board components with their area and marking at 1st pin. In addition, there are other useful functions. Use the menu, **Tools > Component Arrangement Plan**.

Refer to the Component Arrangement Plan manual for detail instructions.




6. PCB Data Extractor

As a powerful documentation function, using this function, user can export PCB information into MS/Excel file. Target information may be nets, components and their relating properties. Use the menu, Tools > PCB Data Extractor.

Selec C Placed ECAD Net Na ECAD FootPr Packag Functi Device Proper Refere Compo Pin Na Pin Lo	t Extract D omponent I Layer(T/B Rotation Ari ame for Ear Part Name ge Name on Name e Name rty ence Count ponent Heigl me) ngle ch Pin		>	Net Reference N Part Name Reference L Pin Q'ty	lame ocation (2)					
Compackage Compackage Proper Referee Compose Proper Na Pin Lo	omponent I Layer(T/B) Rotation Ari ame for Eac Part Name ge Name on Name Name Name Name rty ence Count ponent Heigl me) ngle ch Pin ht		>	C Net Reference N Part Name Reference L Pin Q'ty	lame ocation (2)					
Placed ECAD Net Na ECAD FootPr Packag Functi Device Proper Refere Compo Pin Na Pin Lo	I Layer(T/B) Rotation Ar ame for Eac Part Name ge Name on Name Name Name rty ence Count ponent Heigl me) ngle ch Pin ht		>	Reference N Part Name Reference L Pin Q'ty	lame ocation (2)					
Padsta Gate N Proper	cation ack Name Name rty Count			<							
	3) Make B	IOM List			Default/	Reset				
	Sa	ave		Load			Cancel				
PCB D	ata Extractor Re	esult (4)				×					
Defe	ranca Nama D	Dart Name	Poforonce Location	Poforonco Location V	Din O'hr	^		D	C D	E	
0 101	C C		23 300	4 800	2			Reference	Part Name Referen	ce Referen	co Din (
083	0	115/10	23 300	5 800	2		2 1	C82	CLI 5V104123 300	4 800	3
2 084	0	115/10	8 905	2 243	2		3 2	C83	CLL5Y104123.300	5.800	2
004	0	1 10V1	9,700	-18 000	2		4 3	C84	CLL5Y1041 8.905	2.243	2
C05	0	110V1	26 300	0.100	2		5 4	C85	CL10Y1061 9.700	-18.900	2
C103		105015	1 600	9 200	2		6 5	C86	CL10Y106126.300	0.100	2
1 (10)		105015	4 500	5,200	2		7 6	C103	CL05C150. 1.600	9.200	2
C104		105015	-2 000	-17 600	2		8 7	C104 (6)	CL05C150. 4.500	5.900	2
C103		105015	1 050	-10.850	2		9 8	C105	CL05C1502.000	-17.600	2
0 0100		05510	4 330	-19.650	2		10 9	C106	CL05C150. 1.950	-19.850	2
0 0109		LUSPIU	9.220	15 670	2		11 10	C109	CL05F1032 4.220	0.100	2
.1 0113			0.750	-13.0/0	2		12 11	C113	CLL5Y1041 0.750	-15.670	2
	t C	LL5Y10	-0.280	-15.6/0	2	~	13 12	C114	CLL5Y1041-0.280	-15.670	2

- ① At the dialog window, **PCB Data Extractor**, select extraction type between **Net** and
- 2 Component.
- ③ If user selects extraction type, dialog window show properties list at left list-control box. Select properties to be extracted as order to match.
- ④ Pressing button menu, **Make BOM List**, shows table-driven document form.
- 5 User can check the output form.
- 6 Pressing button menu, Export to MS/Excel makes MS/Excel sheet.
- ⑦ Check result document.



7. Extract Decap Data

Decoupling capacitor (By-pass capacitor) is capacitor device which connect power and ground nets for the purpose of making stable power supplying. PollEx PCB has the feature to find them in PCB and make its result into document. Use the menu **Tools > Decap Extractor**.



① Select power nets among list.

- ② Select ground nets among list.
- ③ Selection for all power/ground nets in design.
- ④ Button menu, **Make Data** show list of de-coupling capacitors.



Users can change the color of net(s) to make it easier for exploring PCB design. Use the menu, **Tools** > **Net Color**.



① Select net classification.

Net Type: Net sorting depending on net type. Ex) power/ground/signal **Individual Net**: Net sorting depending on net name. **Composite-net**: Net sorting for composite-nets.

- ② After selecting net(s), use the mouse right button. And at pop-up menu, use **Set Color** to select certain color.
- ③ If checking "T", make transparent selected net status.
- ④ Pressing button menu, **Apply** will apply changing into design.
- ⑤ Save the setting of defined color to file(*NCLR). And to use this change at next design opening, check the Load and OK button.



PollEx PCB extracts report for all nets' length on design. Use the menu, **Tools > Net Length View**.

Net Length Viewer				×	Net Length Viewer			×
Net Name	Net Length	Net Length Exception Pin Area	Attribute	^	Net Name	Net Length	Net Length Exception Pin Area	Attribute 🔺
MCU_ABA0			SIGN	AL	MCU_ABA	59.439	58.889	SIGNAL
SIGN00228			SIGN	AL	SIGN0022	9.263	8.713	SIGNAL
MCU_HDMI_TX0P			SIGN	AL	MCU_HDMI_TX0	41.95	41.788	SIGNAL
MCU_ABA1			SIGN	AL	MCU_ABA	1 60.101	59.551	SIGNAL
MCU_ABA2			SIGN	AL	MCU_ABA	61.724	61.163	SIGNAL
MCU_HDMI_TX1N			SIGN	AL	MCU_HDMI_TX1	42.519	42.319	SIGNAL
SIGN00240			SIGN	AL	SIGN0024	3.893	3.343	SIGNAL
SIGN00241			SIGN	AL	SIGN0024	1 12.096	11.546	SIGNAL
GNDADC			GROUI	ND DI	GNDAD	2.229	1.137	GROUND
SIGN00243			SIGN	AL	SIGN0024	3 8.989	8.356	SIGNAL
VCC1P0_HDMI_PLL			POW	ER	VCC1P0_HDMI_PL	L 2.644	1.652	POWER
SIGN00244			SIGN	AL	SIGN0024	4 9.103	8.553	SIGNAL
SIGN00245			SIGN	AL	SIGN0024	5 66.084	65.056	SIGNAL
SIGN00246			SIGN	AL	SIGN0024	3.309	2.909	SIGNAL
SIGN00247			SIGN	AL	SIGN0024	7 2.693	2.293	SIGNAL
SIGN00248			SIGN	AL	SIGN0024	8 3.45	2.5	SIGNAL
SIGN00249			SIGN	AL	SIGN0024	9 2.557	2.107	SIGNAL
SIGN00231			SIGN	AL	SIGN0023	1 1.083	0.683	SIGNAL
SIGN00232			SIGN	AL	SIGN0023	2 1.145	0.715	SIGNAL
SIGN00233			SIGN	AL	SIGN0023	3 1.869	1.489	SIGNAL
SIGN00234			SIGN	AL	SIGN0023	4 6.799	6.249	SIGNAL
SIGN00235			SIGN	AL	SIGN0023	5 4.451	3.901	SIGNAL
SIGN00236			SIGN	AL	SIGN0023	5 7.806	7.256	SIGNAL
< CTCN00227			CTON	>	< CTCN0022	7 5 1 5/1	4 604	CTCNAL >
C Extractor	All Expor	t MS Excel	et Length Clos	-	C Extractor	All Export	t MS Excel	Net Length Close

* The meaning of **Net Length** is summation of routing pattern's segments. But it does not include the copper pour size. Use the button menu, **Export to Excel** to make list into MS/Excel sheet.



10. Net Analyzer

PollEx PCB makes report for net length analyzing feature. For total net length, user can extract report for segment length on certain layers, to the branching points and to the via(s). Use the menu, **Tools > Net Analyzer**.

Net Analyzer					- 0	×
1 Net Element Node Type	Not Namo	Lawor	Total Longth	NODEL	NODE2	
Component C Branch C Branch & Via	MCU AA2	Layer	62.547	U204::U1	11204::11205	
Alati anath Disalau Tura		1	021017	15.77	1.131	1
Zivet Length Display Type		2				
Vidth Vidth All Node Combinate	n	3				
Transmission Line Type Todudo Via Longth		4		12.52	28.177	7
a loit		5				
30110		6		18.035		
CInch CMil Ccm ©mm CMicroM	MCU_AA3		60.173	U204::U1	U204::U205	
Search Rese	+ 1	1		14.014	1.131	L
	·	2				
V Net Name Active Port	^	4		14,494	28.434	4
☐ MCU_AA12 U204_N7 ▼		5				-
☐ MCU_AA13 U204_T3 ▼		6		17.159		
□ MCU AA14 U204 T7 -	MCU_AA4		61.698	U204::U1	U204::U205	
✓ MCU AA2 U204 P3 ▼		1		2.538	1.131	L
		2				
		3		10.537	24.759	2
		4				
IV MCU_AA5 U2U4_P2 ▼		5		22 025		
✓ MCU_AA6 U204_R8 ▼	MCIL AA5	0	59 756	11204-111	11204-11205	
□ MCU_AA7 U204_R2 ▼	1100_1110	1	55.750	12.315	1.131	
☐ MCU_AA8 U204_T8 ▼		2				-
☐ MCU_AA9 U204_R3		3				
□ MCU_ABA0 U204_M2 ▼	~	4		12.641	27.845	5
	1	5				~
Close	<				>	• /

1	Select element type to make nodes.
	Comp: Net length among components.
	Branch: Net length among components and branching points.
	Branch & Via: Net length among components, branching points and vias.
2	Net Length Display Type: Select desirable objects in report.
	Layer: Shows length depending on layer.
	Width: Shows routing pattern's width.
	All Node Combination: Shows all combinations of nodes.
	Layer Full Display: Shows stack-up information and each layer's length.
	Pin No : Shows components' pin number also.
	Transmission Line Type: Shows transmission line type, not Layer.
	Include Via Length: Shows including via length.
3	Select unit.

- ④ Select target net(s).
- 5 Press **Analyze** button will make analyzing report for selected target net(s).
- 6 Press **Export to Excel** button will make report to MS/Excel sheet.

11. Change Net Name

In case of Zuken Board Designer Interface, it is possible to change the net name of PCB layout from

> Change Net Name.				
*.ruf file. It can be changed on	PDBB. Only same pir	n connection will be cl	hanged. Use the	menu, Tools

Change Net Name		×
Import *.ruf file		
File Path		
ОК	Cancel	

12. Thermal Resistance Calculator

Can calculate thermal resistance value of given material by "Thermal conductivity". Select the shape of target material among circle, square, rectangle, and then give each value for Xdimension (mm) and Y-dimension (mm), Length (mm). Thermal resistance is inversely proportional to area and proportional to length.

Thermal Resistance Calculator	×
Cross-Section	1
Shape Circle X-dimension (mm) 0 Y-dimension (mm) 0	
Length (mm) 0	
Material AIR Thermal conductivity(W/m.K) 0.0265	
Calulated thermal resistance (K/W) 0	ī
Close	

13. Gerber Transformation

After importing Gerber data, and then user can move or mirror the location of it. To use this menu, go to **Tools > Gerber Transformation.**



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Layer	Name
op-metal.phd ottom-metal.phd	1
Mirror C X Mirror	C Y Mirror
Rotation Rotation Angle	0
Move	
x 0	Y 0
✓ Object Select	Move
C Gerber Obj	ect
C CAD Object	t
	rher Laver
5 Remove Ge	Der Layer

- 1 Layer Name: Lists up the Gerber layers. Select the target layer on here.
- 2 Mirror: Shows the mirrored Gerber data.
- ③ **Rotation:** Shows the rotated Gerber data.
- Move: Enter the X and Y coordinates to move the Gerber data.
 Object Select Move: Calculates the coordinate difference between Gerber and PCB data.
 Gerber Object: Select Gerber Object on the screen, and select the object of the PCB data (the location is to move the Gerber data.).
 CAD Object: Select the PCB object on the screen and select the object of Gerber data (the

location is to move the PCB data).

- **5 Remove Gerber Layer:** Deletes the Gerber Layer.
- 6 **Apply:** The settings are reflected on the screen.

14. Visual Layer Composition

User can layer pairs to be displayed at same time. To make layer pairs(composition), use the menu, **Tools > Visual Layer Composition**.



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rtw	ork La	yer l	List				Visual Layer Composition
	No 1	1 2 3 4 5 6 7 8 9 9 10 11 12 13 14 15 16 17 18	Name padstack top Resist-A Symbol-A Symbol-A-1 MetalMask-A HeightLimit-A inhibit(plc)-A inhibit(plc)-C inhibit(wir)-A 6 padstack bottom Resist-B Symbol-B Symbol-B-1 MetalMask-B HeightLimit-B inhibit(plc)-8	Comment PAD_TOP Resist-A Symbol-A-1 MetalMask-A HeightLimit- inhibit(plc)-A inhibit(plc)-A inhibit(plc)-G PAD_BOTTO Resist-B Symbol-B Symbol-B-1 MetalMask-B HeightLimit- inhibit(plc)-E	A 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	2	Visual Layer Name BTM Pad + Pattern (3) Name 6 padstack bottom (4) Add/Edit Delete Visual Layer List Name Comment (5) TOP Pad + Pattern 1, 2 BTM Pad + Pattern 11, 12
-					-		Delete Reset 🕜 Save Load

- 1 Select layers to be included in certain layer composition.
- 2 Pressing this button means selected item will be potential target nets. Selected layers will be copied to the list in **Visual Layer Composition** window.
- ③ Give the name of (layer) composition.
- ④ **Add/Edit** button will make new layer composition item. And, show it in **Visual Layer List** window.
- 5 At **Visual Layer List** contains current layer composition list.
- 6 **OK** button will complete task.
- ⑦ Save button will save current setting into the file, *.vls. In other design, PollEx PCB will load this setting for reviewing design.



* Users can see this layer composition in Layer Set-up window with artwork layer order list. See the



15. BOM Changer

BOM Changer can be substituted for part name as part name in the BOM file. It can be modified to match each other by utilizing Reference Names between the PDB Data and BOM file. Use the menu, **Tools > BOM Changer**.



РСВ



BOM File Pa	ath c+\temp\t	Altair-PollEy WP	alley BOMWPalley BOM vis	v					
	e. in relip in								
EBI File Pat	th C:₩Temp₩/	C:\Temp\Altair-PollEx\PollEx_BOM\test_BOM.EBI							
					NEXT				
BOM List	Part	Туре	Stock ID	Description					
C101	CC3293-7468	Capacitor	ECJ1VB1A684K	0.68uF,10V,+-1	0%				
C102	CC3292-0680	Capacitor	RM216B11H681KA01	680pF,50V,+-10	0%				
C103	CC3293-7510	Capacitor	ECJGVB1C105K	1.0uF, 16V, +-10	0%	L			
C104	CC3293-7510	Capacitor	ECJGVB1C105K	1.0uF, 16V, +-10	0%				
C105	CC3291-2101	Capacitor	RM1882C1H101JA01	100pF,50V,+-5	1%				
D101	CD3135-2101	Diode	DCC010-TB	Io=100mA,P=20	DmW				
D102	CD3137-0056	Diode	RD5.6M-T1B-B2	Vz=5.6V					
D103	CD3135-2015	Diode	DSD015-TB	Io=150mA,P=20	DmW				
D104	CD3135-2015	Diode	DSD015-TB	Io=150mA,P=20	DmW	F			
(⁻	052024-0020	T-a di caban	COLA TOOK	1-11 : 100/ T	140	١			

- 1 Select BOM file(*.xls) and EBI file. And press Next button.
- $\ensuremath{\textcircled{}}$ The contents of BOM file is displayed.
- ③ In case of this option is checked, if the reference name is matched with PCB Data and BOM, it will be listed. In case of this option is un-checked, if the reference name and ECAD part name are matched with PCB Data and BOM, it will be listed.

	Reference Name	Part Name	ECAD Part Name	TYPE	Stock ID	Description	Target ID
	C103	CL05C150JB5NNND	CL05C150JB5NNND	Capacitor	ECJGVB1C105K	1.0uF, 16V, +-10%	Capacitor
	C104	CL05C150JB5NNND	CL05C150JB5NNND	Capacitor	ECJGVB1C105K	1.0uF, 16V, +-10%	Capacitor
~	C105	CL05C150JB5NNND	CL05C150JB5NNND	Capacitor	RM1882C1H101JA01	100pF,50V,+-5%	Capacitor
~	R101	RC1005J000CS	RC1005J000CS	Resistor	ERJ6GEYJ222V	2.2K, 1/8W, +-5%	Resistor
~	R 102	RC1005J000CS	RC1005J000CS	Resistor	ERJ6GEYJ180V	18,1/8W,+-5%	Resistor
	R 103	RC1005J000CS	RC1005J000CS	Resistor	ERJ6GEYJ101V	100,1/8W,+-5%	Resistor
	R104	RC1005J103CS	RC1005J103CS	Resistor	ERJ6GEYJ103V	10K, 1/8W, +-5%	Resistor
	R105	RC1005J103CS	RC1005J103CS	Resistor	ERJ6GEYJ101V	100,1/8W,+-5%	Resistor
	R 106	RC1005J000CS	RC1005J000CS	Resistor	ERJ6GEYJ823V	8.2K,1/8W,+-5%	Resistor
	R107	RC1005J101CS	RC1005J101CS	Resistor	ERJ6GEYJ103V	10K, 1/8W, +-5%	Resistor
	R 108	RC1005J000CS	RC1005J000CS	Resistor	ERJ6GEYJ103V	10K, 1/8W, +-5%	Resistor
	R 109	RC1005J103CS_B	RC1005J103CS	Resistor	ERJ6GEYJ103V	10K, 1/8W, +-5%	Resistor
	R110	RC1005J101CS	RC1005J101CS	Resistor	ERJ6GEYJ330V	330,1/8W,+-5%	Resistor

④ Set **Target ID** of BOM to replace the part name of the PDB Data.

- 5 Check the list to change.
- \bigcirc Press $\mbox{\bf Apply}$ button. Then the result will be pop-up.



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Change List 7			×
Reference Name	Part Name	ECAD Part Name	Target ID
C105	CL05C150JB5NNND	CL05C150JB5NNND	Capacitor
R101	RC1005J000CS	RC1005J000CS	Resistor
R102	RC1005J000CS	RC1005J000CS	Resistor
J			
		Numeri di	OK Cancel

⑦ Show the changed list. Replace the ECAD part name of the PDB as Target ID. And press "OK" button.

PollExPC	В	×
	Original design will b proceed "Ok" or "Cane	e changed. cel"?
	8 OK	Cancel

8 If pressing "OK" button, apply ECAD part name of PDB will be changed. If pressing "Cancel" button, return to the previous status.

16. Worksheet Planner

Use the menu, **Tools > Worksheet Planner**. Refer to the **Worksheet Planner** manual for detail instructions.

17. Golden Sample

Use the menu, **Tools > Golden Sample**. Refer to the **Golden Sample** manual for detail instructions.

18. Compare GDSII

Use the menu, **Tools > Compare GDSII**. Refer to the **Compare GDSII** manual for detail instructions.

Analysis



- 1. Signal Integrity
- 2. Power Integrity
- 3. Radiated Emission
- 4. Thermal

For above features, refer to individual manual for those products.

Option

PollEx PCB supports different viewers for reviewing objects on board. And it has communication toolset with which engineers in remote location can share their idea with watching same screen.

	Opti	ion	<u>Manufacture</u>	Red-mark	Н
1		Par	rt Viewer		
2		Rea	al PCB Assembly	Viewer	
3		Ne	t 2D/3D Viewer	Ĩ.	
4	2	Pad	dstack/Via View	er	
5	E	Ne	t Topology Viev	wer	
		DF	M		•
		DF	E		•
		DF	E+		۲
		DF	A		۲
		DF	x Core Running		
6		Att	tribute Finder		•

- ① Part Viewer
- 2 Real PCB Assembly Viewer
- ③ Net 2D/3D Viewer
- ④ Padstack/Via Viewer
- 5 Net Topology Viewer
- 6 Attribute Finder

1. Part Viewer

Part Viewer is viewer for part library used in current design. It also shows used padstack type and padstack size. Used the menu, **Option > Part Viewer**.





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PCB

2 Part Viewer	– – ×
File View Tool	
	Part List
	All Parts List (2)
	Search Search Search
	No Part Name ECAD N: 4
	7 CLOSE103ZB5NNF CLOSE10
	8 CL05X105MR3LNI CL05X10
	9 47151-0001 47151-0
	10 675031020-BF-Ch 6750310
	11 CIC05P121NC_B CIC05P1
	12 CIM05F750NC CIM05F7
	13 CIC05P121NC CIC05P1
	14 BSS123 BSS123
	15 RC1005J000CS RC1005
	16 RC1005J103CS RC1005J
	17 RC1005J102CS RC1005J
	18 RC1005J104CS RC1005J
	19 RC1005J103CS_B RC1005J
	20 RC1005J515CS RC1005L
	21 RC1005J105CS RC1005J
	22 RC1005J223CS RC1005
	23 RC1005J220CS RC1005L
	24 RC1005J202CS RC1005J
	25 RC1005J101CS RC1005L
	26 RC1005J432CS_B RC1005J
	2/ RC1005J4/2CS_B RC1005.
	28 RC1005J2R2C5_B RC1005
	29 RC1005J201CS_B RC1005J
	30 KC1003J2K2C5 KC1003
	31 EGGGE 13101 EGGGE 32 PC10051330CS B PC10051
	32 RC1005550C5_8 RC1005
	34 ST1185S ST1185
	Origin Change 3
	X: 0 Y: 0 Change
	To Center To First Pin
	Q Q X 4
	4 View/Edit Part Attributes
	-0.21, +2.87

- 1 At main window's left side, there is part's shape.
- 2 At searching box, user can input keyword and find part.
- ③ At main window red line crossed point means origin points of part. User can change the origin of part.



④ **View/Edit Part Attributes** button menu give users to check more detail information of part. After pressing this button, user can meet following picture's window.

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PCB

2 Part Viewer	- 🗆 X
	Part View Edit
	Lib Part No. 14
	Part Name BSS123
	ECAD Part Name BSS123
Δ	Device Name BSS123
	Package Name SOT23
	Footprint Name SOT23
	Attribute
	Comp Height C
	Mount Type OTHER
3 276	Comment
5.220	uver : 1 A
	· · · · · · · · · · · · · · · · · · ·
	Reference List
	01 TOP -4,900 1
	Q2 TOP 1.000 1
1.000	6
⊲───── 3.000 ────►	
Vin Edit Jum Name Cat Tuna Dad Name Legatia Legatia Medel Tuna Medel Tina Medel Name	
1 1 1 BID V SS1 0 R90 T 0 0 NONE V V	
2 2 2 BID V SS1.0_R90_T 7 1.905 0 NONE V V	•
3 3 3 BID V SR1.27-0.914_R90_T 0.9525 2.0914 NONE V	Measure 8
	Comp Pad Silk S/R M/M
	٩ ٩ 🔍
	Back to Parts Index
Apply	

- **5 Component Name Field** contains different identifiers assign to part.
- 6 At this window, it shows referenced components list.
- \bigcirc For pins used by part, this window shows whole properties of used pins.
- ⑧ Using various buttons in Measure tab, user can make displaying dimensions for component size, pad size, silk, solder/metal mask size.
- * Next is another way to invoke Part Viewer in other tools in PollEx PCB. Upon linking with other tools, user can use Part Viewer much easier.
- 1) Using **Part Viewer** in **Picking Tool**.



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- ⑨ Upon launching picking tool, after selecting components list, using mouse right button, run a pop-up menu.
- 0 And, among the menus, select Run Part Viewer.
- ① **Part Viewer** will be launched.

2) Using Part Viewer in PCB Explorer.



¹² Upon launching **PCB Explorer**, at component list window, select component.

③ And use the menu, **Option > Part Viewer**. **Part Viewer** with selected part will be launched.



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Real PCB Assembly Viewer connects the PCB design data and 3D UPF library to create 3D PCB shapes and export them as 3D common data like *.stp and *.stl.

2.1. 3D UPF Library Link

Before using the Real PCB Assembly Viewer, users need to link 3D package libraries with PCB design.

① Run **Properties > Parts** menu.

<u>F</u> ile	<u>S</u> ett	ting	<u>V</u> iew	<u>P</u> ro	perties	I	ools	<u>A</u> nalysis
			2.		Nets			
	-				Compo	site	Nets	;
					Net Cla	isse	s	
					Net Bu	ise	/Grou	ips
					Parts			
					Compo	ne	nts	
					Materia	al Li	brary	
					Layer S	Sta	ck	

② Click the button "..." to set the UPF library path. If user sets the default part library directory in the environment setting (Setting > Environment > General), the user does not need to set it.

		Refere 🔨	Thermal	Electrical	Package	Pin	Passive	Functional Type	Package	Footprint	Name	Name
2			For Folder	Browse		Counc	Value				0	v
				Line of the		23			HDMI-01D	HDMI-01D	*	51-0001
		/	rary Director	UPF Libr		5			USB-MICRO-5P	USB-MICRO-5P	*	031020
		_				2			XT-32.768	XT-32.768	*	8T-32.768KHZ
^		UPFs				4			XTAL-ISC32	XTAL-ISC32	¥	1-16MHZ
	7151-0001	47				2			PAD2P-1.0X1.0	PAD2P-1.0X1.0	Ŧ	T_MODE
	8037-2100	48				3			SOT23	SOT23	Ŧ	123
	75031020	67				2			FB1005	FB1005-3PCB	Ŧ	5P121NC
	B38T-32.768KHZ	A				2			RES1005	RES1005	*	5F750NC
	SFL1-16MHZ	A				2			CL1005	CL1005-2PCB	*	5C150JB5NNNI
		B				2			CL1005	CL1005-2PCB	Ψ	C270JB5NNW
	050125					2			CL1005	CL1005-2PCB	Ŧ	F103ZB5NNN
	M05E750N C					2			CL1005	CL1005-2PCB	v	X105MR3LNN
~			_			2			CL1608	CL1608-5PCB	Ψ	Y106MQ8NRM
			UPFs	Folder:		2			CL1005	CL1005-2PCB	*	Y104MQ3NLN
	_			_		2			R-CHP-2125	R-CHP-2125-F	Ψ	GEYJ101
Cancel	ОК		New Folder	Make		96			IC-BGA96/K4B4G1	IC-BGA96/K4B4G1	-	Q4G63AFR
		U1	-			513			IC-NXP4330	IC-BGA-513P	*	XP4330
		V				-						

③ Click **Synchronize** button to display the UPF library setting information on each part. Click **Close** button to close the **Parts** dialog.



Part Name CPN) ∇	UPF Name (MPN)		Footprint	Package	Functional Type	Passive Value	Pin Count	Package	Electrical	Thermal	Refere
C1005J000CS	RC1005J000CS	•	R1005-2PCB	R1005	Resistor	Variable	2	(- (h)-		R1,R1(
C1005F241CS	RC1005F241CS	•	R1005-2PCB	R1005	Resistor	Variable	2	(R231,F
C-NXP4330	IC-NXP4330	•	IC-BGA-513P	IC-NXP4330	Digital IC	NXP4330	513	(- Co-		U1
15TQ4G63AFR	H5TQ4G63AFR	•	IC-BGA96/K4B4G1	IC-BGA96/K4B4G1	Capacitor	Variable	96	(U204,l
RJ6GEYJ101	ERJ6GEYJ101	•	R-CHP-2125-F	R-CHP-2125	Resistor	Variable	2	(-10-		R226,F
CLL5Y104MQ3NLN	CLL5Y104MQ3NLNC	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C82,C8
L10Y106MQ8NRM	CL10Y106MQ8NRNC	•	CL1608-5PCB	CL1608	Capacitor	Variable	2	(C85,C8
L05X105MR3LNN	CL05X105MR3LNNH	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C220,0
L05F103ZB5NNN	CL05F103ZB5NNNC	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C109,0
L05C270JB5NNW	CL05C270JB5NNWC	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C116
CL05C150JB5NNNI	CL05C150JB5NNND	•	CL1005-2PCB	CL1005	Capacitor	Variable	2	(C103,0
CIM05F750NC	CIM05F750NC	•	RES1005	RES1005	Other	75	2	(FL1,FL
CIC05P121NC	CIC05P121NC	•	FB1005-3PCB	FB1005	Capacitor	Variable	2	(FB3,FB
SS123	BSS123	•	SOT23	SOT23	Discrete		3	(Q1,Q2
OOT_MODE	BOOT_MODE	•	PAD2P-1.0X1.0	PAD2P-1.0X1.0	Other		2	(Т3
SFL1-16MHZ	ASFL1-16MHZ	•	XTAL-ISC32	XTAL-ISC32	Other		4	(X101
B38T-32.768KHZ	AB38T-32.768KHZ	•	XT-32.768	XT-32.768	Other		2	(X102
Link Part library directory	/ C:\Temp\Altair-Po	llEx	**************************************								>
MPN Reference file	C:\Users\jaehyun	₩A	ppData₩Roaming₩A	Itair₩PollEx₩Data₩	MPN_Reference.xls						

2.2. Real PCB Assembly Viewer

Run Option > Real PCB Assembly Viewer menu.





① Export to 3D Data

3D shaped PCB generated from the Real PCB Assembly Viewer can be exported to 3D common formats. Supported formats are *.stp and *.stl.

2 Exit

Click Exit menu to close the Real PCB Assembly Viewer.

2.3.1.	Export 1	to	3D	Data
--------	----------	----	----	------



Export to 3D Option

- ① Type
- ② Option
- ③ Board
- ④ Layer
- 5 Export



2.3.1.1. Type Specify the 3D data type to export.

Export 3D Option		×
Type (* STEP	⊂ sπ.	C IDF

2.3.1.2. Option

Set options for exporting as 3D data.

Se	ect Component
Metal Mask	
Top Layer	E Bottom Layer
Net (Export Selected N	ets only)
	Select Net
 Footprint Pad Export as separate fi 	Include Board Geometry ile per Net
Roard	
sckage	
Body	Lead of Pin
Footprint	Board Figure
Solder Resist	Silkscreen
Include Drill Layer	
Include Drill Layer yer tart Layer 1 nd Layer 6	•
Include Drill Layer ayer tart Layer 1 nd Layer 6 Exception	•
Include Drill Layer ver tart Layer 1 nd Layer 6 Exception Component Net	• • •
Include Drill Layer ayer tart Layer I Component Net Component DB File	
Include Drill Layer aver tart Layer 1 nd Layer 6 Exception Component Net © Component DB File © Direct Select from	
Include Drill Layer Include Drill Layer Itart Layer I Include Prill Layer I Include Drill Layer I Include Drill Layer I Include Drill Layer I I Pin Component	
Include Drill Layer Include Drill Layer Itart Layer I Ind Layer Exception Component Net Component DB File C Direct Select from Display Name Criteria I	✓ ✓
Include Drill Layer Include Drill Layer Include Drill Layer Include I I I I I I I I I I I I I I I I I I I	✓ ↓ ✓ Component List it by: © Part © Reference Search
Include Drill Layer Include Drill Layer Include Drill Layer Int Layer Ind Layer 6 Exception Component Net © Component DB File O Direct Select from Display Name Criteria Search S Part Name CUSY10400	
Include Drill Layer Include Drill Layer Int Layer Int Layer Exception Component Net Component DB File C Direct Select from Display Name Criteria S Part Name CLLSY104MQ CLLSY104MQ CLLSY104MQ	Component List Component List t by: © Part © Reference Search Footprint Name N3NLNC CL1005-2PCB SaNLNC, CL1005-2PCB
Include Drill Layer Include Drill Layer Itart Layer I Include Drill I	✓ ✓
	Component List Component List Component List Footprint Name SanLNC CL1005-2PCB SanNNC CL1005-2PCB SanNNC CL1005-2PCB SanNNC CL1005-2PCB
	Component List Component



2.3.1.2.1. **Component (Export selected components by each file)**: Option to export the selected components used in the design data with 3D shape.



2.3.1.2.2. **Metal Mask**: Metal Mask drawn as positive on the PCB design data is converted into negative and exported as 3D data. User should set the Metal Mask thickness in the layer setting.



- 2.3.1.2.3. **Net(Export Selected Nets only)**: Option to export the selected Net as 3D data.
- **Footprint Pad**: Export including the footprint pad which connected to the net.
- **Include Board Geometry**: Export including the PCB board shape.





2.3.1.2.4. **Board**: Option to export the shapes of the board and components in the design data.



- -. Package: Select whether to export package Body and Lead of Pin.
- -. Footprint: Select whether to export part footprint.
- -. Board Figure: Select whether to export the board figure drawing in the PDB design data.
- -. Solder Resist: Select whether to export the solder resist.
- -. Silkscreen: Select whether to export the silkscreen.
- -. Route: Select whether to export the routing.
 - **Except Copper**: Option to exclude the copper-pour.



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-. Layer: Set the range of layers to be exported.

Start Layer: Set the start layer.

End Layer: Set the end layer.

-. Exception: Option to exclude components and nets.

Component: Select the components to be excluded from the list or use the Component DB(*.txt) file.

omp	oonent Net		4	1
c 0	Component DB File		23	
• D	Wrect Select from Compor	vent List		_
1	1 Pin Component			
Displ	ay Name Criteria by:	(Part C	Reference	æ
Sear	dh 🛛		Search	S.,
s	Part Name	Footprint Na	me	~
	CLL5Y104MQ3NLNG	CL1005-2PC	3	11
7	CLL5Y104MQ3NLNG	CL1005-2PC	3	
7	CL10Y106MQ8NRN	CL1608-5PC	3	
7	CL05C150JB5NNND	CL1005-2PCE	3	
~	CL05F103ZB5NNNC	CL1005-2PC	3	1
	CL05C2703B5NNWC	CL1005-2PC	3	
	CL05F103ZB5NNNC	CL1005-2PC	3	
	CL05X105MR3LNNH	CL1005-2PC8	3	
	47151-0001	HDMI-01D		¥
	47101-0001	110111-010		

Net: Select the nets to be excluded from the list.

Sear	dh 🛛	Sear	ch
s	Net Name	Net Type	1
Г	MCU_ABA0	Single-ended signal	1
	SIGN00228	Single-ended signal	
	MCU_HDMI_TX0P	Diff Signal +	
Г	MCU_ABA1	Single-ended signal	
	MCU_ABA2	Single-ended signal	
Г	MCU_HDMI_TX1N	Diff Signal -	
Г	SIGN00240	Single-ended signal	
Г	SIGN00241	Single-ended signal	
V	GNDADC	Ground	
Г	SIGN00243	Single-ended signal	
Г	VCC1P0_HDMI_PLL	Power	
	SIGN00244	Single-ended signal	
Г	SIGN00245	Single-ended signal	
Г	SIGN00246	Single-ended signal	
Γ	SIGN00247	Single-ended signal	
	SIGN00248	Sinnle-ended sinnal	۷

2.3.1.3. Board

Select the board to export from the list if there are multiple boards in the PCB design data like the Panel PCB.

C Dened Minister Hardet		4		Board Layer	Option
S Board Width Heigr	t	Height	Width	Board	S
Board_0 63.6	65	63.6		Board_0	P



2.3.1.4. Layer Set the thickness of the PCB board.

No.	Name	Thickness(mm)	
1	1	0.035	
-	Dielectric Laver	0.065	
2	2	0.035	
-	Dielectric Layer	0.15	
3	3	0.035	
	Dielectric Layer	0.15	
4	4	0.035	
	Dielectric Layer	0.15	
5	5	0.035	
	Dielectric Layer	0.065	
5	6	0.035	
Bo	ard Total thicknes	s (mm) 0.79	
So	lder thickness (mr) 0	
si	k thickness (mm)	0	
M	tal thickness (mm)	0	
1.16	con a new less (min)	· · · ·	

-. Table

No.: Display the physical layer number.

Name: Display the layer name.

Thickness(mm): Display the thickness of the layer. The displayed value can be modified by double-clicking it.

-. Board Total thickness(mm): If checked this option, the thickness of layers specified above is ignored and user can define the total thickness of the board.

Solder thickness (mm): Set the thickness of the solder resist.

Silk thickness (mm): Set the thickness of the silk.

Metal thickness (mm): Set the thickness of the metal mask.





Set the export path.

•	•						
Browse For Folder		×					
Export Path							
>	PollEx_RedmarkPlus	^					
>	PollEx_SI						
>	PollEx_Thermal						
~	project_PollEx_New_Sample						
	> 📙 Part						
	> Signal_Integrity						
>	Signal_Integrity						
>	UPFs						
>	UPFs-old						
> 📙 Us	ers	~					
Eolder: project_PollEx_New_Sample							
Make New Folder	OK Cano	:el					

2.4. View



- $\textcircled{1} \quad \text{Component}$
- 2 Route
- ③ Board Outline
- ④ Constrain Axis
- 5 Toggle Axis Cross
- 6 Zoom In
- ⑦ Zoom Out
- ⑧ Zoom 1:1
- 9 Color Setting
- 10 Show Solder Resist





- ① General View: Display only PCB shape except 3D components.
- 2 **PCB Assembled View**: Display both PCB shape and 3D components.
- ③ **Toggle On/Off**: Select whether to display per component reference in the list.

2	Ref. Name			^
~	C82			
~	C83			
7	C84			
7	C85			
◄	C86			
~	C103			
~	C104			
✓	C105			
◄	C106			
~	C109			
~	C113			
4	C114			
~	C116			
2	C121			
2	C122			
~	C123			
	+			
ear	n			

④ Lead On/Off: Select whether to display the component lead.

2.4.2. Route

Option to turn on or off the 3D PCB geometry.



Route Display Off

Route Display On

2.4.3. Board Outline

Option to turn on or off the board outline display, only when the width value is drawn more than 0.



2.4.4. Constrain Axis

Option to limit the rotation axis.

Fix Ax	×					
Сx	Сх Сү					
	Close					

2.4.5. Toggle Axis Cross

Option to turn on or off the display of XYZ axis pivot.



2.4.6. Zoom In/Out Option to zoom in or out.

2.4.7. Zoom 1:1 Restore the display to default.

2.4.8. Color Setting





2.4.9. Show Solder Resist

The solder mask designed as positive in PCB design data is converted to negative to display the solder resist layer as much as the input thickness.





2.5. Tools

This item provides convenient functions such as measuring distance between parts and cutting board view.



- ① Component List
- 2 Measure
- ③ Board X/Y Cut
- ④ Create 3D Geometry by using Component Outline

2.5.1. Component List

Search the parts used in the design.



- 2.5.1.1. Information: Export information of components in the PCB design.
 - ① **Total**: The total number of components used in the PCB design.
 - ② **Registered package geometry**: The number of components with the 3D geometry registered in the UPE library.
 - ③ **Unregistered package geometry**: The number of components with the 3D geometry not registered in the UPE library.
 - ④ **Search**: Search components by Part Name or Reference Name.
- 2.5.1.2. Part/Reference Table: List of components used in the PCB design can be checked the information. The component is highlighted in red when selected a component from the list.



										р	.137
Pa	rt Re	eference	4	⊳		Part	Re	ference		4	⊳
М	. 3D	Part Name	Footprint Name	^)	м	3D	Referenc	Part Name	Footprint Name	^
	章	ERJ6GEYJ101	R-CHP-2125-F]		Ŵ	C82	CLL5Y104MQ3NLNC	CL1005-2PCB	
	审	RC1005J330CS	R1005-2PCB				-	C83	CLL5Y104MQ3NLNC	CL1005-2PCB	
	章	RC1005F241CS	R1005-2PCB				-	C84	CLL5Y104MQ3NLNC	CL1005-2PCB	
22	章	ST1185S	SW-CTT1135				-	C85	CL10Y106MQ8NRNC	CL1608-5PCB	
333	1	BOOT_MODE	PAD2P-1.0X1.0			878	-	C86	CL10Y106MQ8NRNC	CL1608-5PCB	
		TP-C	PIN-Q1			809	÷.	C103	CL05C150JB5NNND	CL1005-2PCB	
		TP-C	PIN-Q1			888	-	C104	CL05C150JB5NNND	CL1005-2PCB	
823	輸	IC-NXP4330	IC-BGA-513P			999 (Ŕ	C105	CL05C150JB5NNND	CL1005-2PCB	
	-	H5TQ4G63AFR	IC-BGA96/K4B4G1646B-SAMSUM			888	-	C106	CL05C150JB5NNND	CL1005-2PCB	
	1	ASFL1-16MHZ	XTAL-ISC32			888	-	C109	CL05F103ZB5NNNC	CL1005-2PCB	
	1	AB38T-32.768KHZ	XT-32.768			878	-	C113	CLL5Y104MO3NLNC	CL1005-2PCB	-
	1	1060	1060	~			T.				~

2.5.1.3. Property: Check the property information of selected component.

2.5.2. Measure

This menu measures the distance between components.



- ① **Body to Body**: Measure the closest distance between the bodies. The measured value can be checked in **Property**.
- ② **Body to Lead**: Measure the closest distance between the body and lead. The measured value can be checked in **Property**.
- ③ **Lead to Lead**: Measure the closest distance between the leads. The measured value can be checked in **Property**.

2.5.3. Board X/Y Cut Check the PCB cutting surface.



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2.5.3.1. Slice Plane: Select the X or Y axis of the cut plane.





2.5.3.2. Scroll: Move the selected cutting plane by moving the slider scroll.



- 1 **Slider Offset**: Slide bar moves by the Slider Offset value.
- \bigcirc **X**, **Y**: Indicate the X, Y coordinates of the cutting plane.
- ③ **Pick Location**: Specify the cutting plane location by clicking the desired location.
- ④ **2D View (Lock 3D Rotation)**: Display the cutting surface in 2D.
- **Display across Vias**: Select whether to display Vias in the cutting plane.
- 6 Allow component cutting: Select whether to cut the component.
- ⑦ Through Via, Blind Via, Buried Via: Select whether to display per via type.

2.5.4. Create 3D Geometry by using Component Outline

3D geometry is created by using the COC shape and height information of the component if there is no 3D UPF library.



- ① **All Component**: Generate 3D geometry for all components in the PCB.
- ② **Select Component**: Generate 3D geometry for the selected components from the list.





- ③ **Option**: Option to generate 3D part shape.
 - **COC**: 3D part shape is created based on the component boundary of the footprint.
 - **Maximum Pad area with rectangle shape**: 3D part shape is created based on the largest rectangular area of the footprint pad.
 - Apply COC first if a component has COC.: If a part has a COC (component boundary), 3D part shape is created based on the component boundary of the footprint first. The rest parts which do not have the COC will be created the 3D part shape based on the largest rectangular area of the footprint pad.
 - **Default all component Height**: 3D part shape is created the height of all parts with the entered value.

3. Net 2D/3D Viewer

Net 2D/3D Viewer is viewer for reviewing routing nets on PCB. For net structure, it shows structure with 2D or 3D mode. It also supports for multiple nets. Use the menu, **Option > Net 2D/3D Viewer**.



3.1. Multiple Net Selection Ctrl + Select Net



РСВ



<Net 2D viewer>

- ① Net displaying mode. Select on between **2D View** and **3D View**.
- ② Display Reference Name.
- ③ When user select a net in the list, the zoom status changes according to the net size. if this option is checked, current zoom status will not be changed. But the selected nets will be displayed to that screen.
- ④ Net selection window. Select target net(s).
- 5 Color table for showing each physical layer's color.



<Net 3D viewer>

- 6 Rotation Control in 3D viewing mode.
- Property button will show much detail information for selected net. At new dialog tab, user can see via's location, pattern segment or other net construction structure.



<Net Property>

- 8 **Property** tab contains hierarchical net structure.
- (9) At property dialog tab, user can see detain information. At picture user can check the accurate pin location, component name and pin number.
- 10 Using Net 2D/3D Viewer in Picking Tool.



Upon launching picking tool, after selecting net among list, using mouse right button, run a pop-up menu. Among pop-up menu list, select **Net 2D/3D Viewer**. It will launch viewer for selected net(s).

① Using Net 2D/3D Viewer in PCB Explorer.



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Upon launching "PCB Explorer", at component list window, select component. And use the menu, **Option > Net 2D/3D Viewer.** User can see the launched viewer for selected net.



4. Padstack/Via Viewer

Padstack/Via Viewer is viewer for reviewing padstacks or vias used in parts on active design. Use the menu, **Option > Padstack/Via Viewer**.



- ① Viewer mode selection for padstack or via.
- ② List for padstack or via depending on viewer mode. Upon selecting item in list, viewer will show it shape in 2D or 3D mode. Using 3D mode, user can check each physical layer's pad shape.
- $\ensuremath{\textcircled{}}$ 3 At information tab, there is much detail information for padstack or vias.


4.1. Using Padstack/Via Viewer in Picking Tool.

PollEx, New, Sample pdbb* - Albin PollEx 2020.1 - PCB	– ø ×
Ele Setting View Broperties Iools Analysis Option Hanufacture Bed-mark Help	
i i i i i i i i i i i i i i i i i i i	
	Picking Tool ×
2) Maryla Viewer	Filter
PRIMAWA	Regen Regeneration
Padstack List Vie List	@ All C Segment
Search Search	E Neikhabad Obiert
No Pediata Name	C Concornet C Route
	Distance 0
6 U2745 8807	Dicking Lawar
	- Hong take
	B [Component]
	- Compfigure
	-Route Run Pad/Via Viewer
Pad(Va)Nerre SS10.899 T	-Route - Add to RedMark
Pad(va) Type 500	-Hore Hore to Hourisk
SatEnd Layer	
Hole Type 0	Property
	Pace Layer : TOP Part Name : BSS 123
	Footprint Name : SOT23
	Component Height 1 0.000
RAFE 0.00 0.00	Rotation Angle : 0.000
	Ref-Text Location : - 1.200, 18.650
	Aleriext Holdson Ange : 0.000
	id : Z-17d84f27-7d09-4adc-97b1-ae666de
	<pre></pre>
	useInSchema : Y
	inPartsList : Y partType : NORMAL
	placeRestriction : FREE polarity : PRESENT
	symbolName1:855123
	/
	v .
	< >>
	19.20 MM NUM

- 1 Select objects using picking tool and at picking tool's list, select pin.
- 2 Upon using mouse right button, select menu, **Run Pad/Via Viewer** among menu list.

5. Net Topology Viewer

Net Topology Viewer is net viewer with showing topology style. From the base component pin, to the end connecting elements, this viewer shows all structures and composing elements' information(layer, pattern width, vias...). Use the menu, **Option > Net Topology Viewer**.



Net Topology Analyz	er [MCU_DISD4]						-		×
Net List			MCU DI	SD4					
Search	Search	Reset				2	1 2 3	3 4 5	6
Zoom In Zoom Out	Zoom Box 1:1	1							
Trace Merce Mode		-							
Net Name	Active Port Na	me 🔥							
MCU AODTO	U204 K1	•							
MCU_TCK	U1_AA6	•							
MCU_DISD0	U1_L25	•							
MCU_DISD1	U1_M24	•	MCU_I	DISD4		(4) h			
MCU_DISD2	U1_M25	•	~~~~~	- <u>() [1</u>)-	 		>		
MCU_DISD3	U1_M23	-	U1-M22	W:0.100 L:0.495	W:0.100	W:0.100	27-1		
MCU_DISD4 (1)	U1_M22	•						\sim	
MCU_DISD5	U1_P23	•				L <u>o</u> i	1)	+>	
MCU_DISD6	U1_P24	•				6 W:0.1 L:2.2	100 43	R28-1	
MCU_DISD7	U1_P25	•							
MCU_HOST_USB_ID	U1_C25	•							
SCL_5V	Q1_3	•							
MCU_AA0	U204_N3	•							
MCU_AA1	U204_P7	•							
MCU_AA2	U204_P3	•							
MCU_AA3	U204_N2	•							
MCU_AA4	U204_P8	•							
MCU_AA5	U204_P2	•			 				
Ready	U204 D0	~							

- ① Select the target net in the lists.
- ② Color table shows color of each physical layer. Elements on certain physical layers will be displayed as same color.



③ Base element should be the component's pin. Depending on pin's buffer types, shapes will be different.



- ④ Branching node points.
- 5 Via symbol.
- 6 Routing pattern symbol. It may have information, layer with colors, length and width.

6. Attribute Finder

Make property list for components and their pins. Use the menu, **Option > Attribute Finder**.

6.1. Search Parts Using Pin Pitches

This is searching parts using pin pitches. show pin pitch, pin or reference quantity etc. Also, user can export to excel contents. Click the list, then reference which is matched with selected part name will be highlighted.

PoliEx_New_S	Sample.pdbb* - Altair PoliEx 20	020.1 - PCB										- 0 ×
Ele Setting	View Properties Iools	Analysis Option	Manufacture Be	d-mark Help								
a 🕨 🔒		्र 🖂 🔳 🛢	1, 1	• 🚳	5 6 6		828	1				
												Picking Tool
												Filter
												IF Sik IF Bad Stack / Pe
												M Boute M Egure
												Al C Segment
												T Neighborhood Object
				1.00		20	720					& Component C Route
				~ 100			4- C					Distance 0
					6 al an an		2.1		1.0			Picking Layer
				1.1		60.0 B	1.300		1.1.1			Composed
					litte			• •				CompFigure
					222222	11111 I		_ W				- Pin - Route
				1 - M M.	1000							Route - Via
				1 - A - A	-1000000-	5.31	J. 1000	ed.				- Route - Pad - Figure
				1.00	-		2. 2-1					1000000
				1.00			* * 72	·松田 5555	0.0			
				1 1 1 m	1 hand	LAL	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		18 C			
				100			the inter	-	0.55			
				1.5			B 100	19000	Babo			Property
				1.87			ann in St.	and a state of the				
				1.00	1997	1 7 700		THE DECT. INC	ag 82			
					Total State	16 20	A Harris	New grant				
						A A						
				1.1	1998 25 1 F	* **	165	N 6 73988.				
				1. A. 1. A.	// CT1	200	2001 6					
					2263999	60 18	0000 3	11				
							(<u>1</u>) -					
							•					
						100						
search												X
												_
	Part Name	Pkg/FootPrint	Pin Pitch	Long Pin Pitch	Pin Q'ty	Ref Q'ty	Pad X Size	Pad Y Size	Drill Size	Pin Names		<u>^</u>
1	CLL5Y104MQ3NLNC	CL1005-2PC8	0.9	None	2	10	0.5	0.5	0.0	All Pin		-
2	CLL5Y104MQ3NLN	CL1005-2PCB	0.9	None	2	42	0.5	0.5	0.0	All Pin		
3	CL10Y106MQ8NRNC	CL1608-SPC8	1.6	None	2	2	0.8	0.8	0.0	All Pin		
				_								
Unit (* m	m ⊂mi ⊂1nch							Export MS Ex	cel		OK	
											N N N N N	Tana I Davas I

6.2. Component Attribute

This function is used to find the references matched with selected reference property.

PollEx_View_Sample.pdbb* - Altair PollEx.2020.1 - PC8	- 0
Me Setting Yew Properties Iools Analysis Option Manufacture Bed-mark Heb	
	Picking Tool
	File V Pad Stack
	V Boute V Boute
	P Al C Segnent
	Neighborhood Object
	C Roate
	Poling Layer
	(B) Component
	Pin Pin
	12 9d 900 00 00 00 00 00 00 00 00 00 00 00 00
	No on an a state and a property
	Place Layer : TOP Part Name : HSTQ4G63AFR
	Postprint Name : IC 66496/KBW
	Component Height : 0.000
	Rotation Angle : 270.000 ECAD Rotation Angle : 270.000
	Ref-Text Location : -24.500, 2.00 Ref-Text Rotation Angle : 0.000
	California Comment>
	d 12-3078 1004-4084-47ec-6966-
	wer:3
	usebilayout : Y
	partType : NORMAL placeRestriction : FREE
Lucas ryper Values ryper Value	polarity : PRESENT symbolName 1 : 1C-QFP-96P
Search Rem	
A 10.1 0.00	
Deimter Rem	
	<
(5) Apply To Explorer Export MS Excel OK	•

- ① All of reference property header listed. When you click **Apply** button, the reference name which is matched with selected property header is listed to right list box. If the selected Item is **All list**, all reference property will be displayed.
- ② All value of selected header in ① listed. If you select one of list and click **Apply** button, the reference name which is matched with selected property header and value is listed to right list box
- ③ Enter the value of selected property header in ① to find. And click **Apply** button, the reference name which is matched with selected property header and value is listed to right list box
- ④ Enter the delimiter to separate the value based on input string.
- 5 Apply and to explorer or export to excel.



Red-mark

Red-Mark is a function to make comment on design. To leave message or comments for purpose to send task, this function will be used efficiently.

<u>F</u> ile	<u>S</u> etting	<u>V</u> iew	Properties	<u>T</u> ools	<u>A</u> nalysis	<u>O</u> ption	<u>M</u> anufacture	<u>R</u> ed-mark	<u>H</u> elp	
		2.	% 📐 🗔	1 🖂	3 🖬	📧 🐲	🗑 🚮 1. 1	Red-m	nark	
		20	V	0 ~0	~ =			Red-m	ark Plus 🔹 🕨	

1. Red-mark

During exploring PCB design, if user input red-mark comment and save, all red-marks will be saved into PDBB file. So later, when other engineer open the design file, it is possible to see added red-mark comments. Use the menu, **Red-mark > Red-mark**.

Red-ma	rk		×		Red-mark ×
List	ontents		4 Þ		List Contents
All			•	(2)	Title Check the value: R221
	Display	All RedMark Area		Ũ	Category 1 Category 2 Category 3
No	Category	Title			Contents
1	1-1	Check the value:	R221 2		Writer Jeunkyoung
				3	- Referenct Name: U1 ^
					Please check the value of R221 which is c
				_	< >
				(4)	Property
					Item Value
				-	Remove Selected Property
					•
					Add Remove
				5	File
					Add Property
					Remove Selected Property
					Add Remove
				6	Add Draw Object
					Width 0.3 Default Color
					Start Type
					End Type
		- L	-		Rectangle Circle Freeform Custom Color
		Delete	Close		Done Cancel
	Save	Load	•		

① Use **Add**, **Del** or **Close** button to add, delete or close red-mark in list, respectively.

- ② Input new red-mark name.
- ③ Add message at this editing tab.
- ④ Add properties.
- 5 Attach file to Red-mark.
- 6 Select drawing object to make geometry into Red-mark. Supporting geometries would be circle, rectangle or arrow. Using geometries supported by **Red-mark**, user can express more easy and intuitive representation.



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- ⑦ After adding Red-mark, user can see list of completed Red-marks.
- 8 Saving PDBB file in PollEx PCB will also save added red-marks into PDBB file.



% When other users open the design, if there are red-marks are attached, PollEx PCB will open them automatically as upper picture.



2. Red-mark Plus

In Red-mark Plus, it is enabled to get the upgrade features for mark-up tools such as drawing object, text, measurement and reply, history etc.

Refer to the **Red-mark Plus** manual for detail instructions.

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