Altair PollEx 2021

Gerber To PCB User Guide

altair.com

Intellectual Property Rights Notice

Copyrights, Trademarks, Trade Secrets, Patents & Third Party Software

Copyrights in the below are held by Altair Engineering, Inc., except where otherwise explicitly stated. This Intellectual Property Rights Notice is exemplary, not exhaustive.

> **Note:** Pre-release versions of Altair software are provided 'as is', without warranty of any kind. Usage of pre-release versions is strictly limited to non-production purposes.

Altair HyperWorks™ - The Platform for Innovation™

Altair AcuConsole™ ©2006-2021

Altair AcuSolve™ ©1997-2021

Altair Activate® ©1989-2021 (formerly solidThinking Activate)

Altair Compose® ©2007-2021 (formerly solidThinking Compose)

Altair ConnectMe™ ©2014-2021

Altair EDEM ©2005-2021 DEM Solutions Ltd, ©2019-2021 Altair Engineering Inc.

Altair ElectroFlo™ ©1992-2021

Altair Embed® ©1989-2021 (formerly solidThinking Embed)

- **Altair Embed SE** ©1989-2021 (formerly solidThinking Embed SE)
- **Altair Embed/Digital Power Designer** ©2012-2021
- **Altair Embed Viewer** ©1996-2021

Altair ESAComp™ ©1992-2021

Altair Feko™ ©1999-2014 Altair Development S.A. (Pty) Ltd., ©2014-2021 Altair Engineering Inc.

Altair Flux™ ©1983-2021

Altair FluxMotor™ ©2017-2021

Altair HyperCrash™ ©2001-2021

Altair HyperGraph™ ©1995-2021

Altair HyperLife™ ©1990-2021

Altair HyperMesh™ ©1990-2021

Altair HyperStudy™ ©1999-2021

Altair HyperView™ ©1999-2021

Altair HyperXtrude™ ©1999-2021

Altair Inspire™ ©2009-2021 including Altair Inspire Motion, Altair Inspire Structures, and Altair Inspire Print3D

Altair Inspire Cast ©2011-2021 (formerly Click2Cast)

Altair Packaged Solution Offerings (PSOs)

Third party software licenses

AcuConsole contains material licensed from Intelligent Light (www.ilight.com) and used by permission.

Software Security Measures:

Altair Engineering Inc. and its subsidiaries and affiliates reserve the right to embed software security mechanisms in the Software for the purpose of detecting the installation and/or use of illegal copies of the Software. The Software may collect and transmit non-proprietary data about those illegal copies. Data collected will not include any customer data created by or used in connection with the Software and will not be provided to any third party, except as may be required by law or legal process or to enforce our rights with respect to the use of any illegal copies of the Software. By using the Software, each user consents to such detection and collection of data, as well as its transmission and use if an illegal copy of the Software is detected. No steps may be taken to avoid or detect the purpose of any such security mechanisms.

Technical Support

Altair provides comprehensive software support via web FAQs, tutorials, training classes, telephone, and e-mail.

Altair One Customer Portal

Altair One (https://altairone.com/) is Altair's customer portal giving you access to product downloads, a Knowledge Base, and customer support. We strongly recommend that all users create an Altair One account and use it as their primary means of requesting technical support.

Once your customer portal account is set up, you can directly get to your support page via this link: www.altair.com/customer-support/

Altair Training Classes

Altair's in-person, online, and self-paced trainings provide hands-on introduction to our products, focusing on overall functionality. Trainings are conducted at our corporate and regional offices or at your facility.

For more information please visit: https://learn.altair.com/

If you are interested in training at your facility, please contact your account manager for more details. If you do not know who your account manager is, please contact your local support office and they will connect you with your account manager.

Telephone and E-mail

If you are unable to contact Altair support via the customer portal, you may reach out to technical support via phone or e-mail. Use the following table as a reference to locate the support office for your region.

When contacting Altair support, please specify the product and version number you are using along with a detailed description of the problem. It is beneficial for the support engineer to know what type of workstation, operating system, RAM, and graphics board you have, so please include that in your communication.

Location	Telephone	E-mail
Australia	+61 649 413 7981	anzsupport@altair.com
Brazil	+55 113 884 0414	br_support@altair.com
Canada	+1 416 447 6463	support@altairengineering.ca
China	+86 400 619 6186	support@altair.com.cn
France	+33 141 33 0992	francesupport@altair.com
Germany	+49 703 162 0822	hwsupport@altair.de
Greece	+30 231 047 3311	eesupport@altair.com

Location	Telephone	E-mail
India	+91 806 629 4500 +1 800 425 0234 (toll free)	support@india.altair.com
Israel		israelsupport@altair.com
Italy	+39 800 905 595	support@altairengineering.it
Japan	+81 36 225 5830	support@altairjp.co.jp
Malaysia	+60 32 742 7890	aseansupport@altair.com
Mexico	+52 555 658 6808	mx-support@altair.com
New Zealand	+64 9 413 7981	anzsupport@altair.com
South Africa	+27 21 831 1500	support@altair.co.za
South Korea	+82 704 050 9200	support@altair.co.kr
Spain	+34 910 810 080	support-spain@altair.com
Sweden	+46 46 460 2828	support@altair.se
United Kingdom	+44 192 646 8600	support@uk.altair.com
United States	+1 248 614 2425	hwsupport@altair.com

If your company is being serviced by an Altair partner, you can find that information on our web site at https://www.altair.com/PartnerSearch/.

See www.altair.com for complete information on Altair, our team, and our products.

Contents

Conventions Used in this Guide

This guide uses the following conventions:

Bold Italic	All commands from the user interface. Options, menus, buttons, and dialog box names are bolded, but not italicized. Example: On the **Welcome** screen, click ***Next***.
`Courier`	The path of a program or folder; a web address; a file name or component; text that the user is expected to enter. Example: The default path is `C:\Program Files\Altair\2019\PollEx`

Questions regarding the document may be directed to PollEx team at PollEx_support_kr@altair.com.

Gerber to PCB

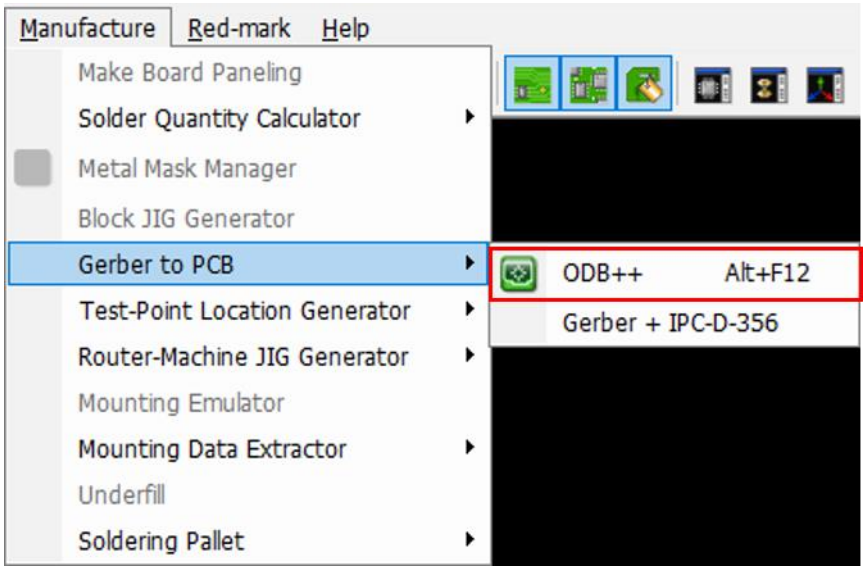
Gerber to PCB is a PCB generator from graphical Gerber or ODB++ file which is non-intelligent data. By importing graphical Gerber or ODB++ file, users can generate it into intelligent PCB design file through the Gerber to PCB.
Gerber to PCB has two features of **ODB++** and **Gerber + IPC-D-356**.

ODB++

The **ODB++** converts a limited ODB++ design file that has only graphical data into PCB.
After converting as the intelligent PCB design, it can be used for the Bare Board Test (BBT), which checks electrical liabilities on the PCB.

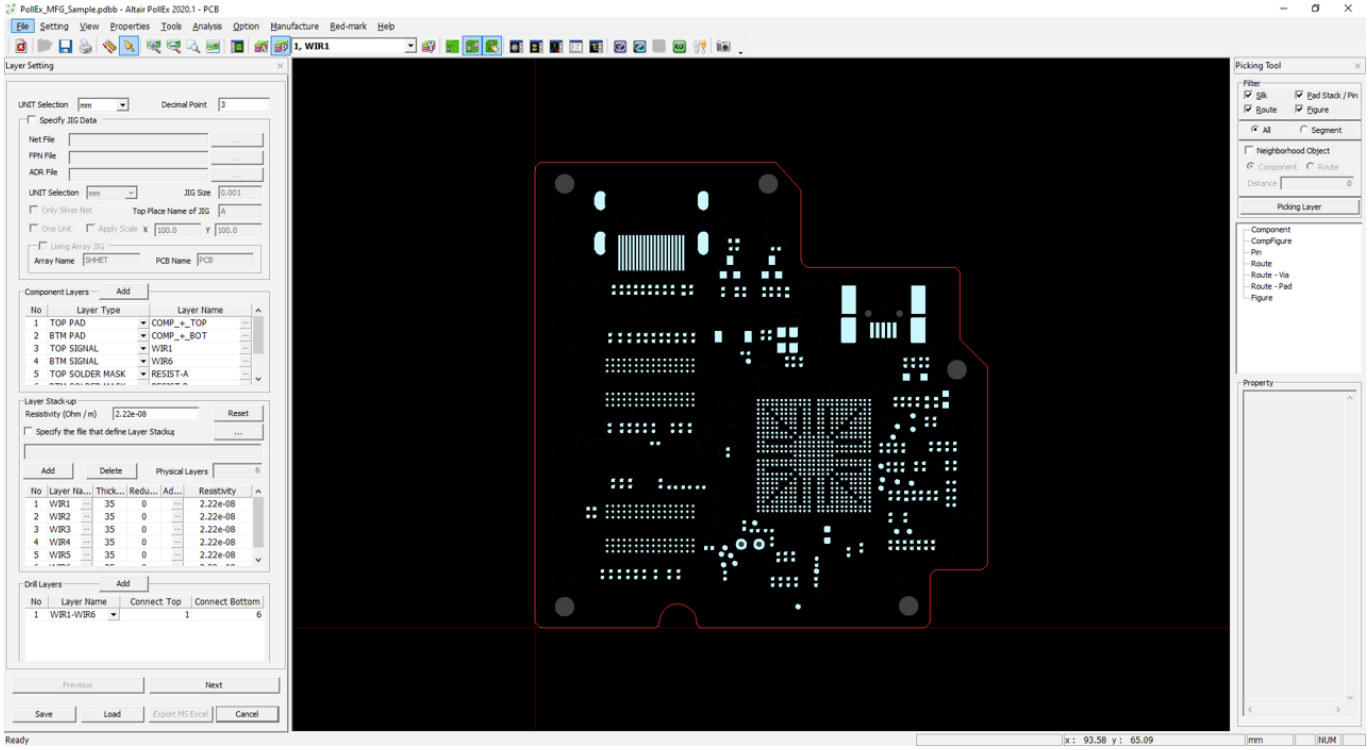
1. Launch ODB++

Gerber to PCB is the optional module of PollEx PCB. After launching the PollEx PCB, Select the menu, **Manufacture – Gerber to PCB – ODB++** or click the icon from the menu bar.
Please note that the menu will not be enabled if you import ODB++ data which includes net data.



2. ODB++ GUI

To make the intelligent PCB design data, users will have four different processes, **Layer Setting**, **Make Component**, **Make Netlist**, and **Result Information**. These dialogs are displayed on the left-side of the main window. By clicking **Previous** or **Next** button, users can move to different dialog.
On the right-side of the main window, the **Picking Tool** dialog is displayed. For more detailed information, please refer to the **PollEx PCB** manual.



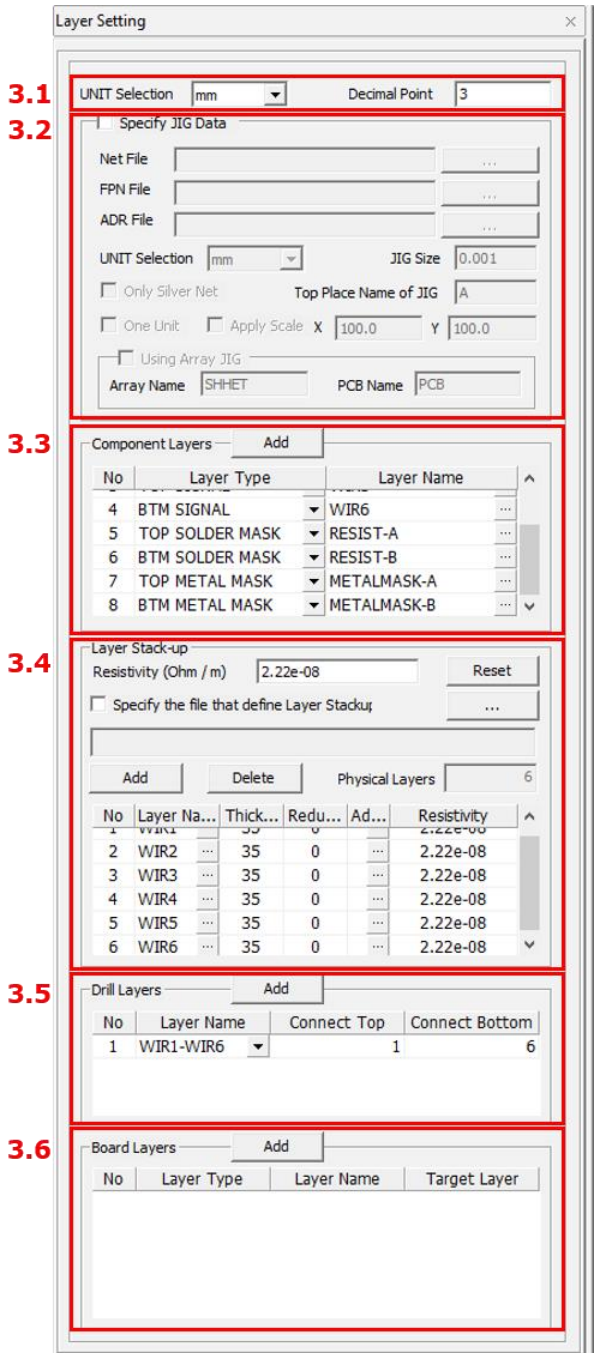
2.1. Save and Load for the environment setup

On the bottom side of each dialog, users can save or load the environment setup.

a. **Save**: The current user setting environment can be saved as `*.pgt` file.
b. **Load**: Users can load the pre-defined setting environment.
c. **Export MS Excel**: After generating PCB design, users can see the result in **Result Information** tab. Users can export the result to MS Excel by using this button.

3. Layer Setting

To generate a PCB design file using ODB++ data, it is required to properly load the necessary files for the layers. When the required data are imported, users need to match the data to create the PCB design file.



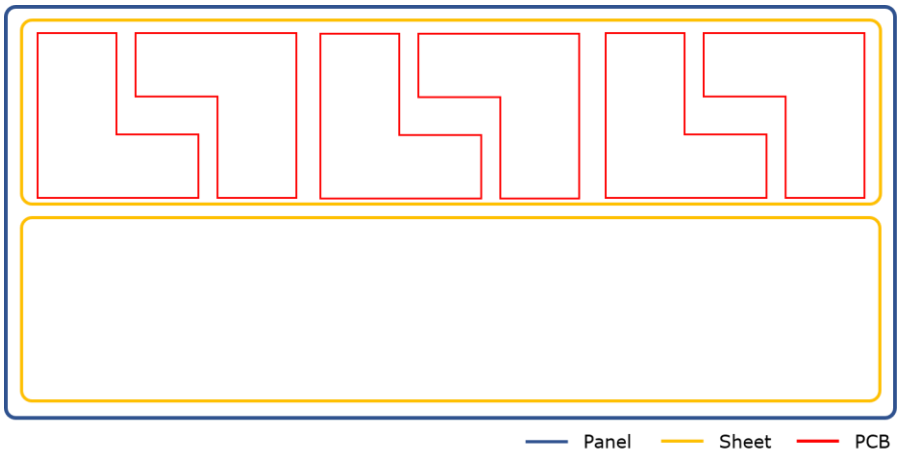
3.1. Unit setup

- **UNIT Selection**: Select a unit.
- **Decimal Point**: Set the decimal point for the coordinates of part and net generation.

3.2. Specify JIG Data

- Net/ FPN/ ADR File: These files are exported from the Bare Board Tester (BBT) with the pin number, pin name, net name, and location.
- UNIT Selection: Select the unit used in the Net, FPN, and ADR files.
- JIG Size: Enter the JIG pin size to be applied.

- Only Silver Net: When this option is checked, checks only 4W pins.
- Top Place Name of JIG: Specify the top placed JIG pin's name in the ADR file.
- One Unit: Check this option when the imported design is a single board.
- Apply Scale: Enter the contraction rate of the produced board.
- Using Array JIG: Specify the Array Name and PCB Name of the imported design. Refer to the name definition for each board as follows.



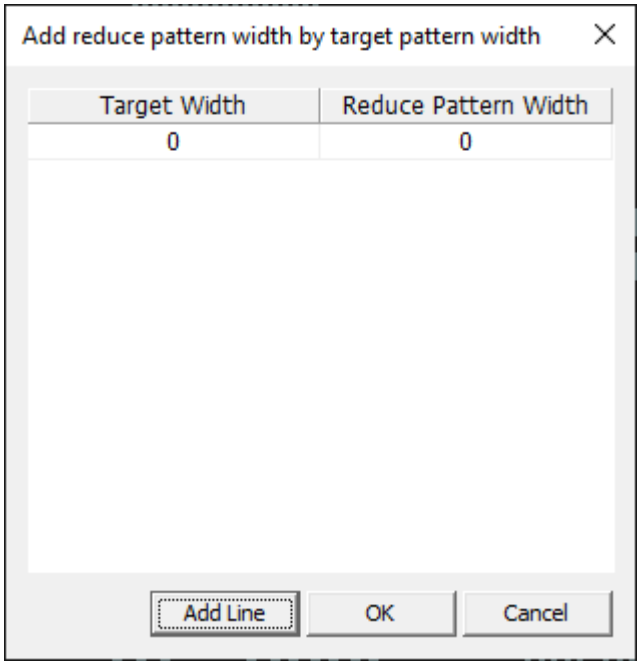
3.3. Component Layers

- **ADD**: By clicking **Add** button, users can add the line.
- **Layer Type**: Specify the layer type, such as Signal, PAD, Solder Mask, and Metal Mask per Top and Bottom.
- **Layer Name**: Specify the layer of imported Gerber of ODB++ data to match with the **Layer Type.**

3.4. Layer Stack-up

- **Resistivity (Ohm/m)**: Enter the resistance value of the material.
- **Reset**: Initialize the **Layer Stack-up** settings.
- **Specify the file that define Layer Stackup**: Import the Excel format file of the layer stack up information.
- **Add**: By clicking **Add** button, users can add a line.
- **Delete**: By clicking **Delete** button, users can delete a line.
- **Physical Layers**: Number of the total physical layers.
- **Layer Name**: Select the layer stacking order as the actual design physical layer.
- **Thickness**: Specify the thickness of the physical layer.
- **Reduce Pattern Width**: Enter the reduced width of the produced route. This input value is reflected in the nominal resistance calculation.

- **Add Reduce Pattern Width**: Specify the reduced pattern width per a target pattern width. This input value is reflected in the nominal resistance calculation.



- **Resistivity**: Enter the resistance value per a layer. This input value is reflected in the nominal resistance calculation.

3.5. Drill Layers

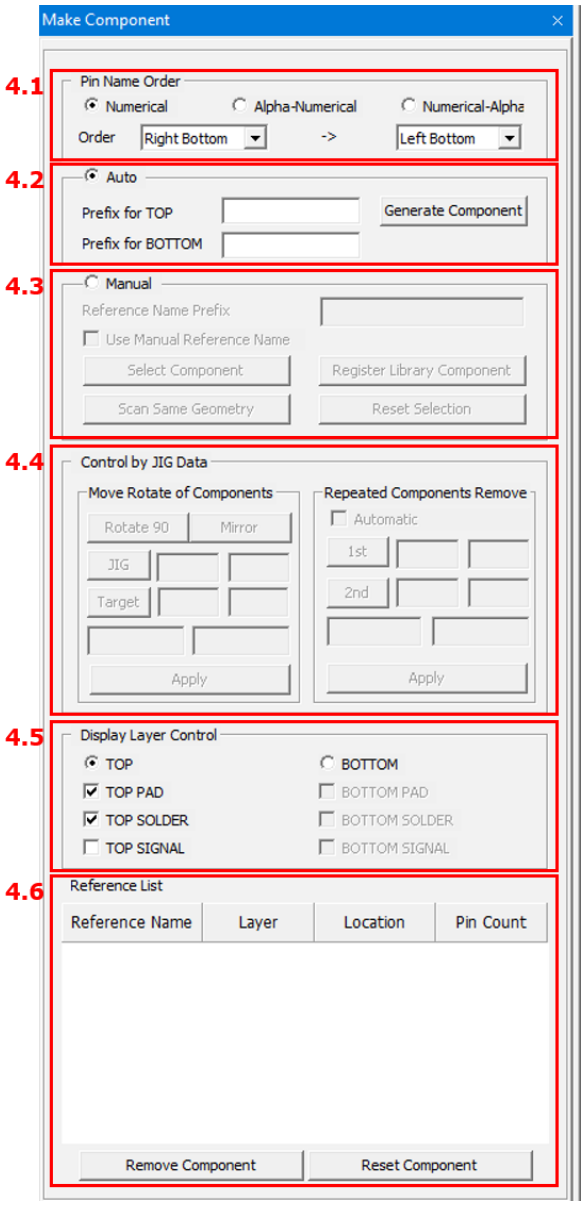
- **Add**: By clicking **Add** button, users can add a line.
- **Layer Name**: Select the drill layer used in the original design data.
- **Connect Top**: Set the start drill layer number.
- **Connect Bottom**: Set the end drill layer number.

3.6. Board Layers

- **Add**: By clicking **Add** button, users can add the line.
- **Layer Type**: Select the layer type either Board Outline or Etch.
- **Layer Name**: Select the layer name corresponding to the layer type.
- **Target Layer**: Select a layer to apply the board layer set in the **Layer Type**.

4. Make Component

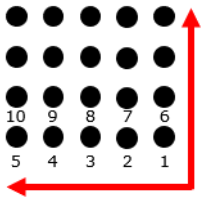
After completing the layer setting, users can create components either automatically or manually.



4.1. Pin Name Order

For creating parts, specify the way of assigning the pin number.

- Numerical: Assign the pin number with a number (ex. 1, 2, 3…).
- Alpha-Numerical: Assign the pin number with an alphabet and a number (ex. A1, A2, A3…).
- Numerical-Alpha: Assign the pin number with a number and an alphabet (ex. 1A, 2A, 3A…).
- Order: Specify the direction of assigning pin number. For example, if users select from Right Bottom to Left Bottom, the pins are assigned like below.



4.2. Auto

The menu creates the parts automatically. Users need to specify the prefix for the Top and Bottom. When clicked the **Generate Component** button, this menu automatically creates the parts for the top and bottom and created parts are listed in the **Reference List**.

4.3. Manual

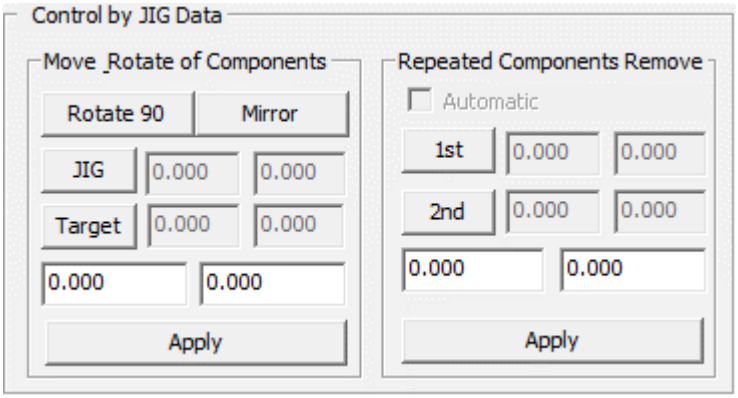
This menu creates the parts manually.

- Reference Name Prefix: Specify the prefix of the parts to be applied.
- Use Manual Reference Name: When this option is checked, users can manually define the reference name for the selected pins instead of the prefix defined in the **Reference Name Prefix**.
- Select Component: Select pins to create as a component with the **Reference Name Prefix**.
- Scan Same Geometry: Find the same components which defined in the **Select Component**.
- Register Library Component: When clicked this option, register the searched parts into library.
- Reset Selection: Reset the selected pins.

4.4. Control by JIG Data

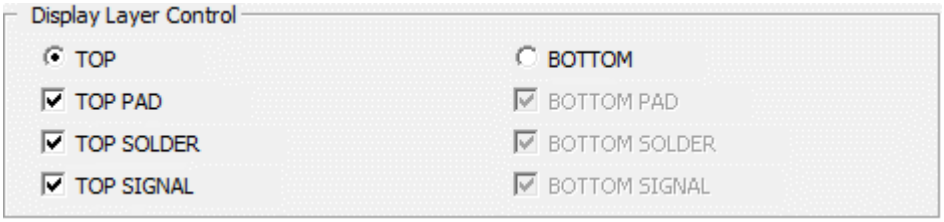
This menu is activated when the user specifies the menu of **Specify JIG Data** in the **Layer Setting**.

- **Move Rotate of Components**: Move or rotate the position of the JIG read from the JIG data.
  Click the **JIG** button and select a pin to be moved or rotated.
  Click the **Target** button and select a location to be moved or manually input the location with X and Y coordinates.
- **Repeated Components Remove**: This menu deletes the duplicated JIG data.



4.5. Display Layer Control

Select the display layer of PAD, Solder, and Signal for the Top and Bottom.



4.6. Reference List

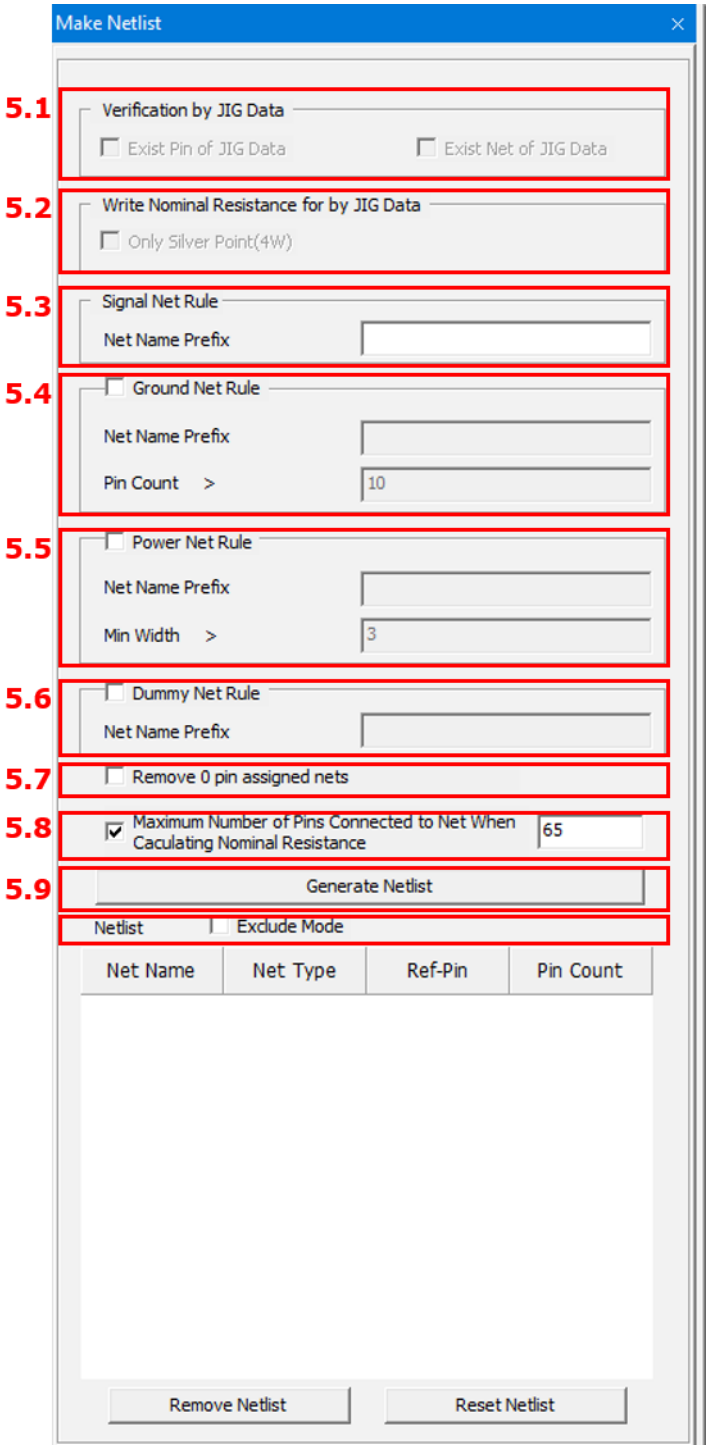
Created parts by automatically or manually are listed in this table.

- Remove Component: Remove the selected components.

- Reset Component: Reset all created components.

5. Make Netlist

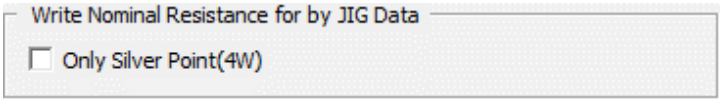
The next step after part creation is that the user can create the routing nets using vias, pins, and patterns. In the **Make Netlist** menu, routing nets can be generated.



5.1. Verification by JIG Data

This menu is activated when the **Specify JIG Data** in the **Layer Setting** is selected. This function is to find differences by comparing JIG data and the design data.

5.2. Write Nominal Resistance for by JIG Data
Calculate the nominal resistance value and save the value in the NET file which is defined in the **Specify JIG Data** of the **Layer Setting**. When the **Only Silver Point (4W)** is checked, only 4W pins of calculated nominal resistance value are saved in the NET file.



5.3. Signal Net Rule
Specify the common signal net prefix.

5.4. Ground Net Rule
Specify the ground net prefix. Nets having more connected pins than the specified **Pin Count** are recognized as the ground net.

5.5. Power Net Rule
Specify the power net prefix. Nets having larger width that the specified **Min Width** are recognized as the power net.

> **Note:** When the **Signal**, **Ground**, and **Power** nets are specified, the ground net condition is searched and set first, then set the power net. The remaining nets are classified as the common signal nets.

5.6. Dummy Net Rule
Specify the dummy net prefix which number of connected pin counts are less than two.

5.7. Remove 0 pin assigned nets
When this option is checked, nets having zero connected pin will not be created as a net.

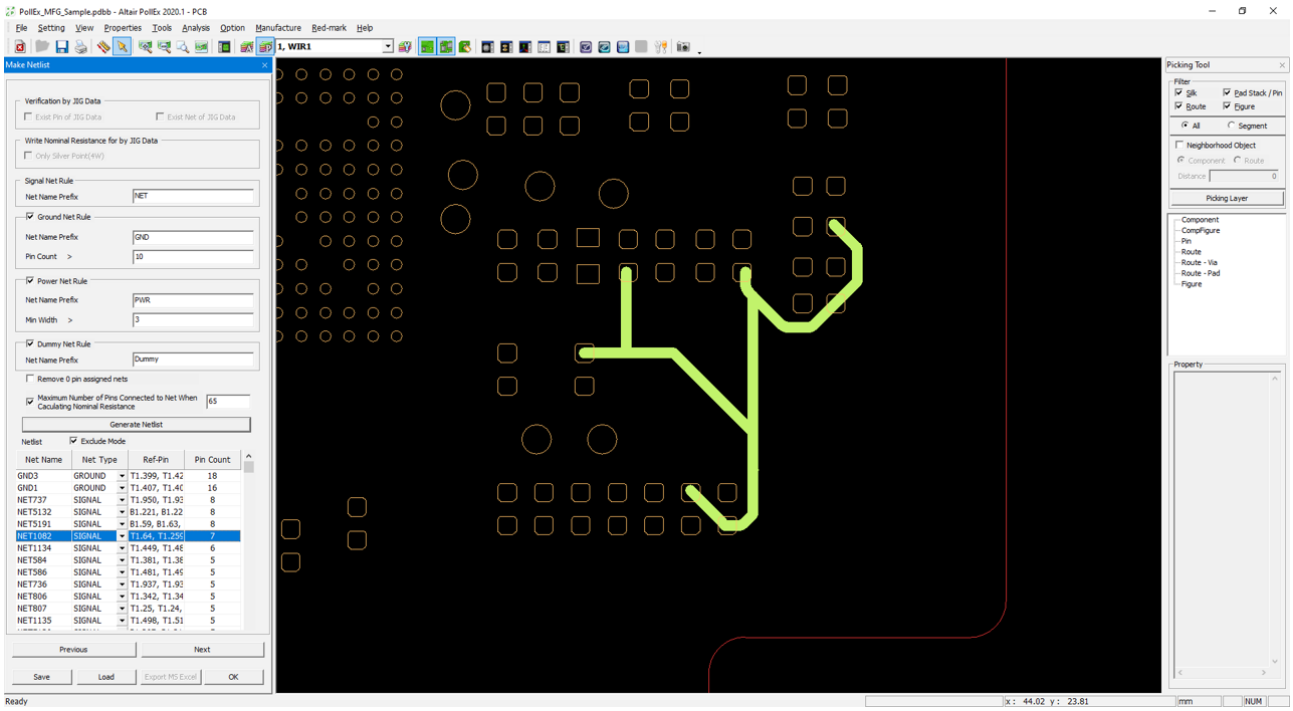
5.8. Maximum Number of Pins Connected to Net When Calculating Nominal Resistance
This option is to exclude nets having more connected pins that the user specified pin counts for the nominal resistance calculation.

5.9. Generate Netlist
When clicked the **Generate Netlist** button, nets are generated with the specified options. The generated nets contain the information of net name, net type, reference pin, and pin count.

Net Name	Net Type	Ref-Pin	Pin Count
GND3	GROUND	T1.399, T1.421, T1	18
GND1	GROUND	T1.407, T1.406, T1	16
NET737	SIGNAL	T1.950, T1.932, T1	8
NET1172	SIGNAL	B1.220, B1.221, B1	8
NET1231	SIGNAL	B1.59, B1.63, B1.51	8
NET1078	SIGNAL	T1.64, T1.259, T1.	7
NET1122	SIGNAL	T1.449, T1.480, T1	6
NET584	SIGNAL	T1.381, T1.382, T1	5
NET585	SIGNAL	T1.481, T1.497, T1	5
NET736	SIGNAL	T1.937, T1.935, T1	5
NET806	SIGNAL	T1.342, T1.341, T1	5

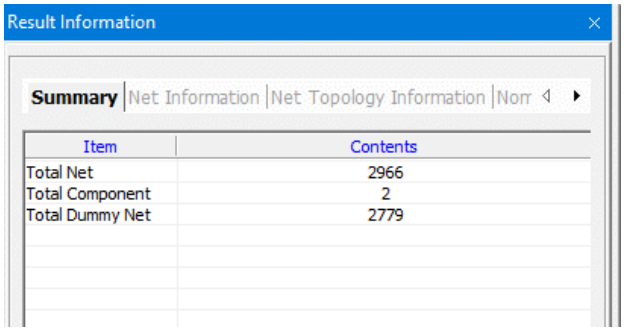
5.10. Exclude Mode

When this option is selected, only selected net from the list is displayed on the right-side.



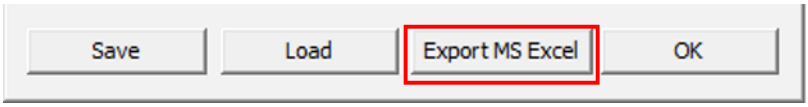
6. Result Information

Once the PCB design generation is completed, users can review the results of four different information of Net, Net Topology, Summary, and Nominal Resistance. On each tab, selected net from the lists will be focused and highlighted on the right-side of window.



6.1. Export to MS Excel

The result information can be exported to MS Excel by clicking the **Export MS Excel** button.



	A	B	C	D	E	F	G	H	I
1	Design File Name : PollEx_MFG_Sample								
2									
3	No	Net Name	Reference.Pin	X	Y	Place Layer			
4	1	Dummy1	T1.1013	19.900	52.700	TOP			
5	2	Dummy3	T1.967	53.900	46.100	TOP			
6	3	Dummy5	T1.965	47.400	41.850	TOP			
7	4	Dummy7	T1.969	35.500	46.700	TOP			
8	5	Dummy9	T1.820	32.050	32.000	TOP			
9	6	Dummy11	T1.818	33.350	32.000	TOP			
10	7	Dummy13	T1.817	34.000	32.000	TOP			
11	8	Dummy15	T1.815	35.300	32.000	TOP			
12	9	Dummy17	T1.812	37.250	32.000	TOP			
13	10	Dummy19	T1.809	39.850	32.000	TOP			
14	11	Dummy21	T1.808	40.500	32.000	TOP			
15	12	Dummy23	T1.807	41.150	32.000	TOP			
16	13	Dummy25	T1.804	43.100	32.000	TOP			
17	14	Dummy27	T1.297	35.950	19.000	TOP			
18	15	Dummy29	T1.295	37.900	19.000	TOP			
19	16	Dummy31	T1.291	41.800	19.000	TOP			
20	17	Dummy33	T1.292	40.500	19.000	TOP			
21	18	Dummy35	T1.288	43.750	19.000	TOP			
22	19	Dummy37	T1.287	45.050	19.000	TOP			
23	20	Dummy39	T1.284	47.000	19.000	TOP			
24	21	Dummy41	T1.278	35.300	18.350	TOP			
25	22	Dummy43	T1.274	38.550	18.350	TOP			
26	23	Dummy45	T1.275	37.900	18.350	TOP			
27	24	Dummy47	T1.268	43.750	18.350	TOP			
28	25	Dummy49	T1.267	44.400	18.350	TOP			
29	26	Dummy51	T1.264	47.000	18.350	TOP			
30	27	Dummy53	T1.247	36.600	17.700	TOP			
31	28	Dummy55	T1.244	39.850	17.700	TOP			
32	29	Dummy57	T1.243	40.500	17.700	TOP			
33	30	Dummy59	T1.236	46.350	17.700	TOP			
34	31	Dummy61	T1.235	47.000	17.700	TOP			
35	32	Dummy63	T1.215	32.050	17.050	TOP			
36	33	Dummy65	T1.211	34.650	17.050	TOP			
37	34	Dummy67	T1.207	37.250	17.050	TOP			
38	35	Dummy69	T1.204	39.850	17.050	TOP			
39	36	Dummy71	T1.203	40.500	17.050	TOP			

Net Information | Net Topology Information | Summary | Nominal Resistance

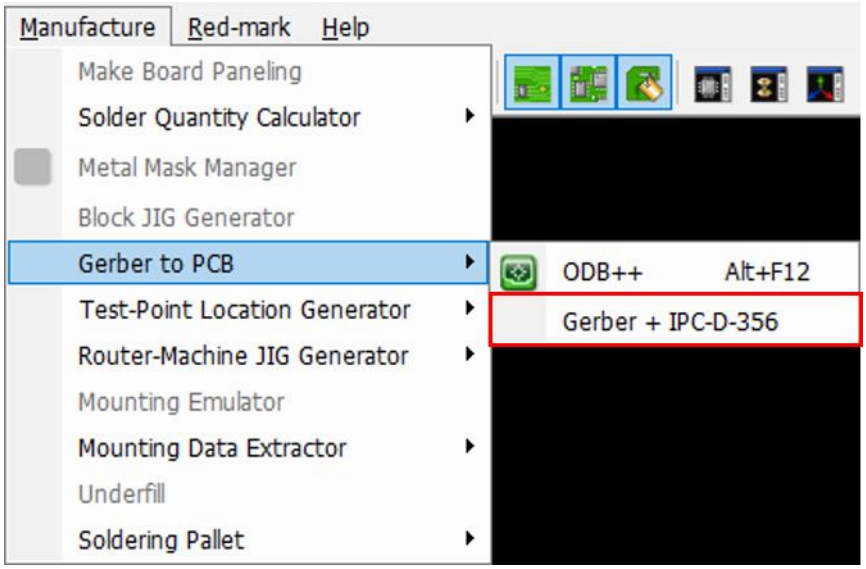
Gerber + IPC-D-356

The **Gerber + IPC-D-356** converts a Gerber design file that has only graphical data into PCB utilizing the IPC-D-356 data by reverse engineering.

1. Launch Gerber + IPC-D-356

Gerber to PCB is the optional module of PollEx PCB. After launching the PollEx PCB, Select the menu, **Manufacture – Gerber to PCB – IPC-D-356** menu.

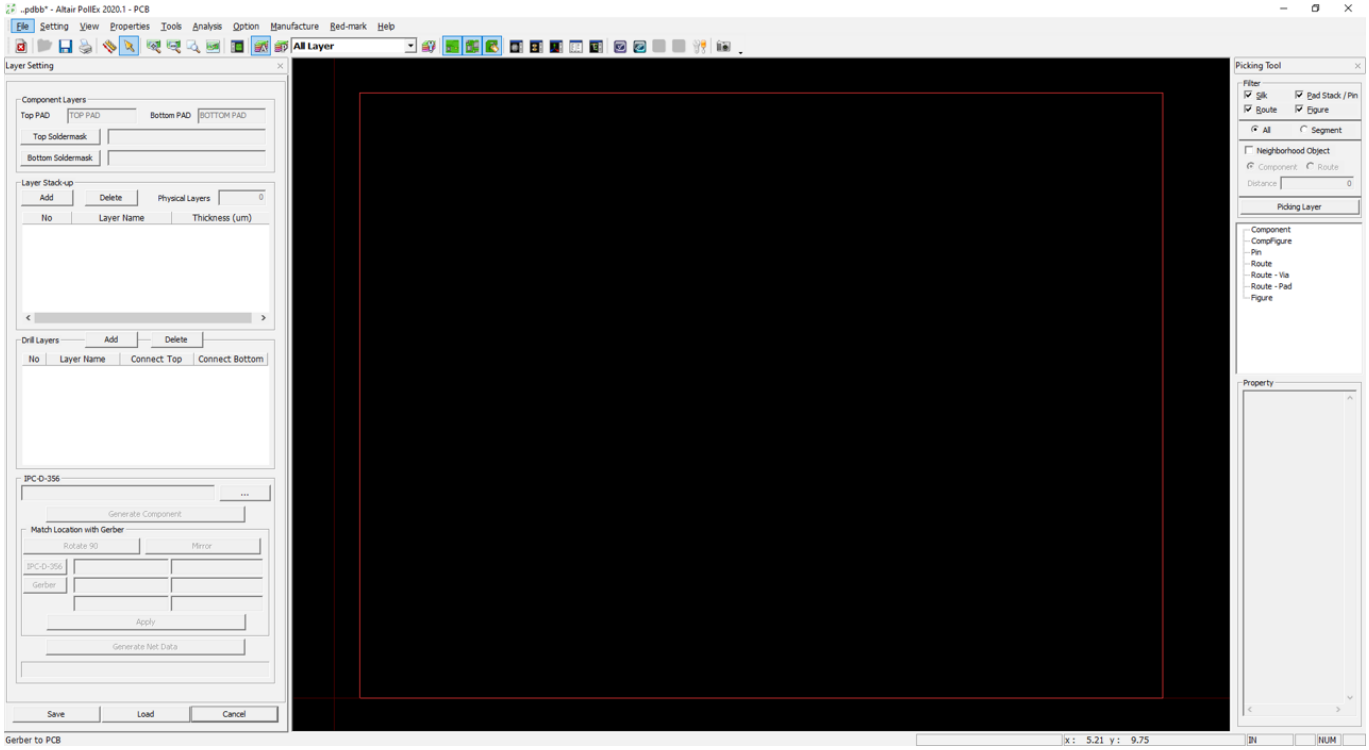
Please note that the menu will not be enabled if you import other than Gerber files.



2. Gerber + IPC-D-356 GUI

To make the intelligent PCB design data, users need to set layers of component, drill, and stack-up. Then, users need to import a IPC-D-356 data and to match the design origin between Gerber and IPC data.

On the right-side of the main window, the **Picking Tool** dialog is displayed. For more detailed information, please refer to the **PollEx PCB** manual.



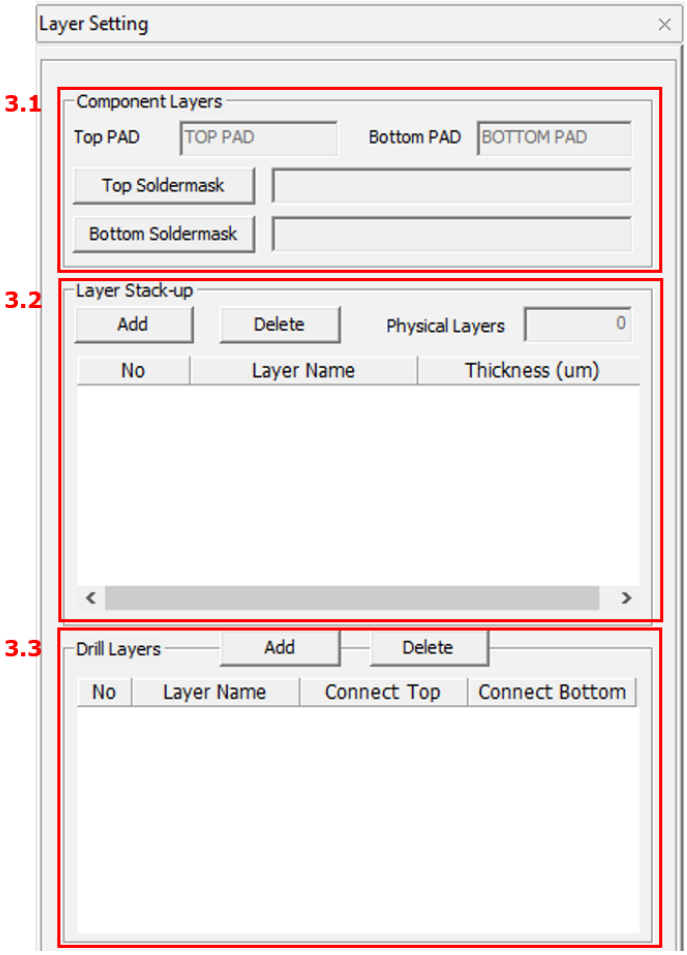
2.1. Save and Load for the environment setup

On the bottom side, users can save or load the environment settings.

a. **Save**: The current user setting environment can be saved as `*.dpce` file.
b. **Load**: Users can load the pre-defined setting environment.

3. Layer Setting

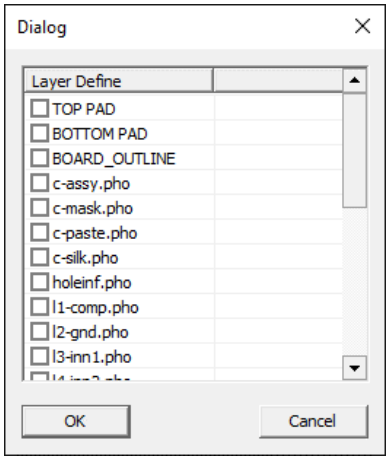
To generate a PCB design file using Gerber files, it is required to properly load the necessary files for the layers. When the data are imported into PollEx PCB, users need to define layers of the Gerber files. When imported Gerber files into PollEx PCB, physical layers are not defined. Imported Gerber files can be viewed in Layer menu. For more details, please refer **Setting - 2.1 Layer** section in PollEx PCB manual.



3.1. Component Layers setup

Top and Bottom PADs are automatically detected.

- **Top Soldermask**: Select the soldermask for the Top layer. When clicked the icon, you can select a layer from the dialog.



- **Bottom Soldermask**: Select the soldermask for the Bottom layer.

3.2. Layer Stack-up setup

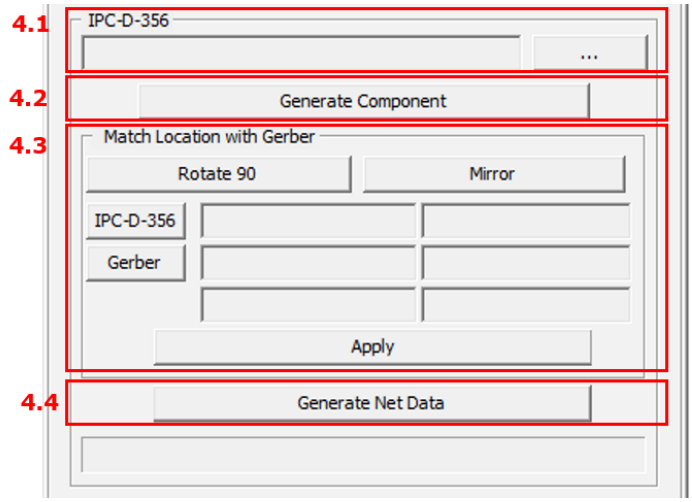
- **Add**: By clicking **Add** button, users can add a line.
- **Delete**: By clicking **Delete** button, users can delete a line.
- **Physical Layers**: Number of the total physical layers.
- **Layer Name**: Select the layer stacking order as the actual design physical layer.
- **Thickness**: Specify the thickness of the physical layer.

3.3. Drill Layers setup

- **Add**: By clicking **Add** button, users can add a line.
- **Layer Name**: Select the drill layer used in the original design data.
- **Connect Top**: Set the start drill layer number.
- **Connect Bottom**: Set the end drill layer number.

4. IPC-D-356

Next step after defined the layer settings is to combine the IPC-D-356 data to generate component and net data. Imported IPC data should be moved (if not matched together).

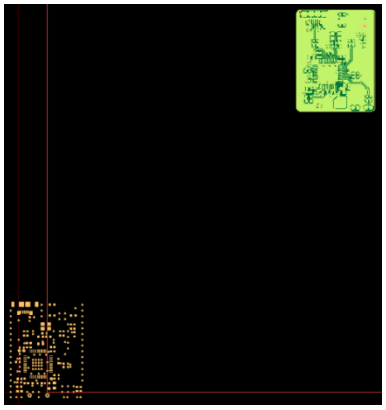


4.1. Load IPC-D-356 data

Select an IPC-D-356 file by clicking the browse button. The supported format is IPC-D-356, IPC-D-356-A, and IPC-D-356-B.

4.2. Generate Component

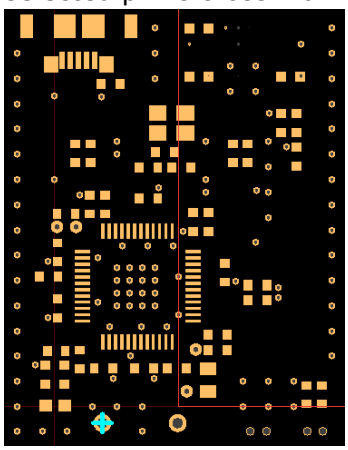
When clicked the **Generate Component** button, pads are displayed on the screen (left bottom on the below figure).



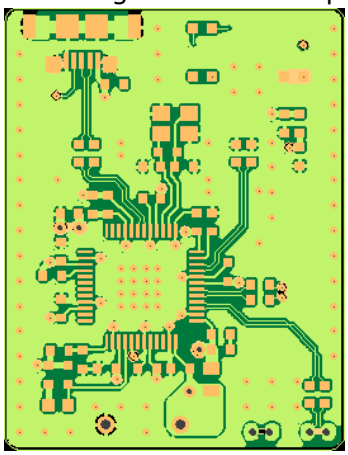
4.3. Match Location with Gerber

For mismatched data, the IPC data should be moved, rotated, or mirrored.

- **Rotate90**: When clicked the button, the IPC data is rotated 90 degrees counterclockwise.
- **Mirror**: When clicked the button, the IPC data is flipped horizontally.
- **IPC-D-356**: Select a reference pin in the IPC data after clicked the **IPC-D-356** button. The selected pin is cross marked. The X and Y coordinates are automatically entered on the table.



- **Gerber**: Select a reference pin in the Gerber data after clicked the **Gerber** button. The X and Y coordinates are automatically entered on the table.
- **Apply**: When clicked the **Apply** button, the IPC data is moved to the Gerber data by matching the reference pin of both data.



4.4. Generate Net Data

This menu is to generate nets to convert as the intelligent PCB data. When clicked the **Generate Net Data** button, the progress bar is displayed the net generating status in the PCB design.

5. Result Information

Once the PCB design generation is completed, users can review the results of three different information of Summary, Net Information, and Net Error Data. On each tab, selected net from the lists will be focused and highlighted on the right-side of window for your review.